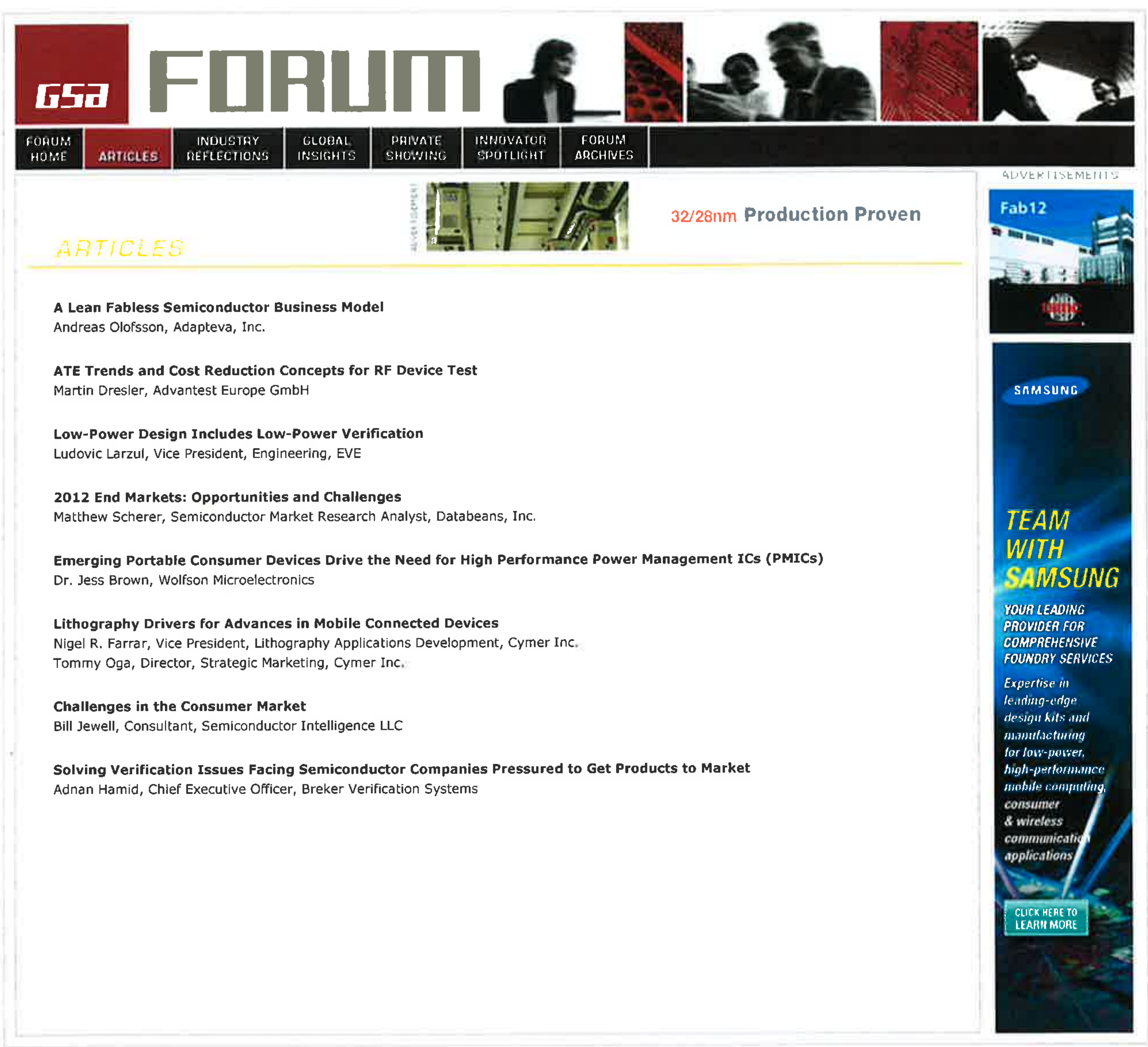

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ATE Trends and Cost Reduction Concepts for RF Device Test

Martin Dresler, Advantest Europe GmbH

The demand for semiconductor devices used in radio frequency (RF) applications like smart phones and wireless local area networks (WLAN) has dramatically increased at an average growth rate of more than 20 percent over the last couple of years. As this demand increases, so too does the speed and capability required of these devices. RF automatic test equipment (ATE) is used for the high-volume production testing of these devices. The instruments of an RF ATE system are more complex than bench equipment, in that the set-up and control of the instruments take place within a highly integrated programming environment. Speed and accuracy are needed in RF ATE systems, because the volume of RF devices tested can be in the millions of units per month. Unit volume and complexity of the RF devices are also growing, as RF standards continue to proliferate. As a result, the RF ATE requirements are also increasing. Smart phones become more capable every year, but are also becoming cheaper and cheaper at the same time. This article will outline the current RF applications trends and discuss cost reduction concepts.

Current RFIC and RF System-on-Chip (SOC) Market Developments

Growth in Unit Volume, Competitive Cost and Time-To-Market Pressure

One main driver in the wireless semiconductor market is handset RFICs, which today generate more than 50 percent of the overall revenue for this market. Handset volumes continue healthy growth and reached 1.6 billion shipments in 2011. At the same time, the RFIC revenue has grown at an average rate of "only" 11 percent per year. The key reason for the disparate RFIC revenue (11 percent) versus handset shipments (20 percent) is the decline of the average selling price by roughly eight percent per year. Examining the iPhone bill of materials and comparing the 3G and 4G components, the RF transceiver device price erosion totaled a stunning 17 percent. This has a direct impact on the progression of device test costs. Typically, the annual cost-of-test (COT) reduction goal is in the range of eight percent.

Besides costs, time-to-market (TTM) becomes a key differentiator. To compete for business for key applications like the iPhone and iPad with steep production ramps and extremely high volumes, it is mandatory for semiconductor suppliers to deliver on time with the requested quality and volume. It is a winner-take-all type of business and timelines must be maintained.

Continued Proliferation of Standards, Integration and Complexity Growth

RF standards continue to proliferate, which implies a broader range of test requirements. In addition to the 2G/3G/4G telephone technologies, modern smart phones contain global positioning systems (GPS), frequency modulation (FM) radio, Bluetooth and WLAN. Signal bandwidth and carrier frequencies supporting higher data rates are steadily increasing, and new standards for wireless communications are expanding mobile handset capabilities at a relentless pace. Some good examples are the evolving WLAN standards 802.11a/b/g, 802.11n and the future 802.11ac with various throughput capabilities, carrier frequencies and bandwidths. In addition, new RF developments need to maintain compatibility with previous standards, enhancing value of both the wireless network and the new technology. As a result, previous generation hardware, which otherwise might have been eliminated by an emerging new standard, is often still required. This has a direct impact on the tester RF pin-count requirements. 3G cellular RF transceivers include both existing quad-band GSM/EDGE standards and dual-/tri-band WCDMA capability. While GSM/EDGE transceivers typically have five or more RF connections, WCDMA with its diversity, can receive channels and add as many as nine additional RF pins, depending on the actual implementation of the RF chip.

RF Integration to SOC and System-In-Package (SIP)

Another trend is the RF integration to SOC and SIP. Higher chip integration helps to reduce manufacturing costs and enables smaller products. The primary focus today is more functionality at an affordable cost and effort. Comparing again the bill of material of iPhone 3G vs. 4G, it becomes apparent that integrating additional RF standards helps to protect the chip price. Today's RFSOC/RFSIP devices incorporate the RF transceiver and digital/analog baseband with integrated power management. While these devices typically target the low-cost market, such as that in China, they add new test challenges. Due to the increased complexity, more tests increase test times. Higher parallelism can be used to counteract the increasing test time, but increasing parallelism for high pin-count RFSOCs forces the tester configuration to 60+ RF ports, together with 1,000+ digital pins and 70+ power supply pins. Need for High Performance and High Quality Test at the Wafer Level Compared to RFSOCs, RFSIPs are more flexible. SIPs offer faster time-to-market due to performance and cost-optimized front-end fabrication processes. However, SIPs add a cost layer from yield loss due to the multiple known good dies (KGDs) attached to the SIP substrate. Any of the dies can induce a failure and need to be tested at wafer level. Another cost reduction trend is the usage of wafer-level chipscale packaging (WLCSP). In this case, the die is mounted on an interposer, upon which pads or balls are formed; or the pads are etched directly onto the silicon wafer, resulting in a small chip package very close to the size of the silicon die. RF test at probe becomes more and more common. This requires not only optimal signal integrity, but also much larger component space on the probe card to allow higher multi-site testing. Using a direct probe solution can enable a single-load board to be used for both wafer probe and final test. This reduces the time between IC development and production, minimizes the correlation effort between probe and final test and enables higher multi-site capability. Octal site RF probe is already a reality today.

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Impact of Market Developments on ATE and RF Test

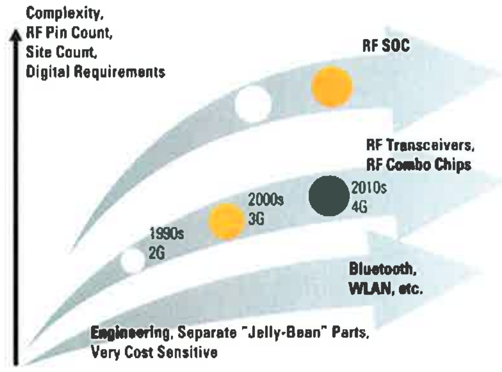
ATE Needs to Cover the Broadest RF Test Needs

The market developments can be summarized as follows: RF unit volume, as well as device complexity are increasing, while product life cycles and average selling prices are decreasing. The standard answer to this challenge so far has been to provide a more complex tester with a more bulky infrastructure to house all the extensive configurations. While this might be necessary for the leading edge and highly integrated RF transceivers and RF SOC devices, it is overkill and too expensive for RF connectivity or combo chips. The additional infrastructure simply adds too much unnecessary cost to the test solution. Depending on the actual configuration, an unsuitable tester infrastructure can add as much as 20 percent to the overall system price. Another 10 percent to 20 percent can be saved, if the tester configuration is matched to the actual application needs.

On the other hand, even low-cost RF devices share the same demodulation requirements, so compromises on tester performance cannot be accepted. Separating and targeting RF ATE platforms for different applications is also not a good choice, because the intersections are floating and quickly changing over time. Today's optimized solution most will likely become obsolete over the lifetime of a device or with its next generation. Switching from one ATE platform to another incompatible platform places a large risk on TTM and will add significant switching costs, which can easily reach into the six-figure range.

A wireless test solution today needs to cover a broader range of devices with different levels of complexity than it did 10 years ago (Figure 1). On the low end, it needs to cover very cost sensitive connectivity devices and front-end modules (FEM), and on the high end it needs to be able to test devices with multiple RF ports, covering a variety of standards combined with mixed signal, digital, power management and embedded or stacked memory testing requirements.

Figure 1: Broadened Complexity of RF Test Needs



Outlining the Architecture of a Scalable and Compatible RF ATE Platform

The need for covering a wide range of applications results in unprecedented asset utilization and manufacturing flexibility. Due to the boundary requirement to have similar RF, analog and digital performance over the full application range, a scalable platform approach provides the best test economics. A scalable platform has consistent operating software, allows exchanging the same hardware modules from one system to the other (digital, analog, RF, etc.) in a choice of compact, small or large test head classes and deviceunder- test (DUT) board reuse; and makes use of the same docking hardware and positioning, therefore enabling a consistent prober and handler set -up over the whole test floor.

The compatible, high-throughput tester classes (Figure 2) must have focus on different RF applications - each with an optimized infrastructure:

- Low-cost infrastructure with focus on dual or quad site testing of low-integration and cost-sensitive RF devices; ultrasmall footprint, ideal for lab development and high-volume production; allows minimum capital cost or hourly rate at outsourced assembly and test (OSAT) companies.
- Low-cost and zero-footprint infrastructure with focus on quad or octal site testing of mid-integration RF devices; allows a high degree of configuration flexibility.
- High parallel test infrastructure for low COT of most complex RFSOC/RFSIP devices; it may need 2,000+ digital pins, 100+ power supply pins and 48+ RF pins.

Figure 2: Scalable RF Platform Can Cover the Full RF Application Spectrum

ATE ($), Hourly Rate ($/H)

Integrated SOC + RF, Quad / Octal Site

Mainstream Mixed Signal/RF, Quad Site

RF Transceiver, Quad / Octal Site

RF Combo / Connectivity

Engineering

Dual / Quad Site

RF Connectivity &FEM

Number and Mixture of Digital, Mixed Signal, DPS, RF

Establishing compatible tester classes will have a significant impact on COT and cost-of-ownership (COO), while eliminating many technology and loading risks. This concept enables semiconductor devices to quickly and easily move from one tester class to another to optimize for lowest cost.

Benefits of a Scalable RF ATE Platform for Low-Cost Applications

A scalable platform has several advantages, especially for the lowend classes. First of all, the same high-performance RF, analog, (high-speed) digital and power supply hardware cards can be used, but the amount of resources needs to be tailored to the needs. Noncritical low-cost applications, like legacy 2G transceivers representing roughly 50 percent of the overall transceiver volume, have typically much

shorter and simpler test lists. In some cases, the index time of the handlers is limiting the throughput. In this case, it is more cost effective to scale down hardware resources and infrastructure to a minimum to achieve the best COT. However, test quality must be maintained. Inaccurate error vector magnitude (EVM) results will lead to yield loss, as well as obsolete voltage and current measurement units. A scalable platform ensures that unexpected test requirements in the low-end have already been solved in the high-end and therefore can be easily leveraged.

The same is true for advanced test techniques. Conventional low-cost ATE for example does not provide mandatory throughput and efficiency features like hidden capture data upload, hidden/ multithreaded calculation and protocol-aware or concurrent test. These benefits can be simply inherited if part of a scalable ATE platform approach. The software is also more powerful. Low-end configurations can leverage the same demodulation library, the same test method library and debug tools. This dramatically improves TTM by reducing training efforts and test program development time. Overall, low-end configurations as part of a scalable RF ATE platform provide best-in-class throughput and usability.

Cost Reduction through Scalability, Compatibility and Innovation

Innovation is the third force that drives cost reduction in addition to scalability and compatibility. Innovation enables new test techniques and higher integration. And without real innovation, only shortdated point solutions are possible. On the other hand, innovative ATE test processors can be as integrated as today's smartphones. They can be implemented in inexpensive CMOS technology and make expensive and large components like field programmable gate arrays (FPGAs) redundant, while performing in the several GHz range. Like other technologies, the same is true for ATE – the higher the integration, the lower the cost. The test processor technology has reached an integration and functionality level that scalable platforms with just a few tester cards can cover the full spectrum from low-cost to high-performance. This is the key economic driver.

The Personal Tester: Benefits of Using Low-Cost Configuration for Engineering and Test Program Development

The legacy approach of test program development is that multiple test engineers share the same test system with a full multi-site production configuration. In a scalable ATE platform environment, using the smallest tester class, with its optimized infrastructure costs, allows the concept of a personal tester. A personal tester would be used by a small team in an engineering or office environment to bring up the single site (or dual site) test program, which typically takes 80 percent of the test program development time, but also quickly handles production escalations (qualification lots, customer samples, pre-production lots). The high-volume manufacturing tester configuration needs to be used only for the last 20 percent, which is the final multi-site tweaking and correlation. Since a real scalable platform is by definition compatible, it is possible to move seamlessly from one tester class to another, dependent on the task. Assuming the engineering configuration has just half the price of the production test system, the engineering fleet could be increased by 66 percent with the same level of ATE investment. This potentially improves TTM by as much as 66 percent, providing more debug time and at the same time higher product quality, faster customer escalation handling and more time for test time reduction.

Summary

Today, a wireless test solution needs to cover an even broader range of devices, with different levels of complexity than a decade ago. This article has shown that overall cost reduction can be only successful, if the platform is scalable, compatible and innovative. A scalable and innovative ATE platform can cover the broad range of requirements to test a variety of wireless devices, thus enabling higher asset utilization and manufacturing flexibility. One aspect of scalability is to provide different compatible tester classes with optimized infrastructure. The low-cost classes especially benefit from scalability. They can inherit all the innovative throughput and usability features, which today's legacy low-cost test solutions cannot provide. This enables low-cost ATE, with best in class usability, throughput and economics.

About the Author

Martin Dresler works at Advantest Europe and has more than 16 years of ATE experience in the areas of mixed-signal, high-speed memory and RF in different positions. As RF market development manager, he is researching new types of businesses, products and services, with an emphasis on identifying current and future opportunities in the mitigation of customer needs. He is a frequent presenter at international conferences and has a university teaching assignment in Stuttgart. He holds a Master (Dipl.-Ing.) of electrical engineering from the Technical University of Munich and a Master (Dipl. Wirt.-Ing.) of business administration from the Fern-University Hagen.