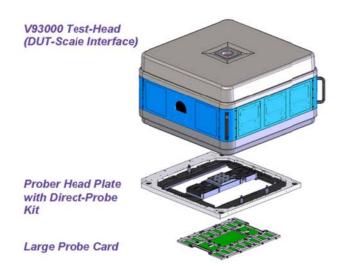


V93000 Direct-Probe™

Solution Overview



High-performance wafer probe test solution for wireless, WLCSP, MPU and GPU devices

Industry Challenges

Mobility, interconnectivity and multimedia are driving ICs toward smaller, ultra-thin packages of stacked chips with more functionality and greater performance. A higher level of chip integration when combined with today's smaller form factors make it increasingly challenging to perform final package test effectively *and* economically. To ensure quality, maximize yield and lower costs, the components of these highly integrated system-in-packages (SIPs) often require knowngood die (KGD) reliability before entering the packaging step. Increasingly these components are being packaged and tested at the wafer level, commonly referred to as wafer level chip scale packages (WLCSPs).

By conducting at wafer stage the testing normally conducted after devices are packaged, many efficiencies are achieved that lower cost of test. Multi-site testing coupled with reduced indexing and faster test times boosts throughput. Failed die can be marked for removal and sometimes repaired ensuring fewer bad die make it to final packaging, increasing yields. In the case of new products and during process ramp, full test results at wafer provide faster feedback to designers and fabricators. The design effort and hardware cost of test setups can be shared between test points, reduced or even eliminated.

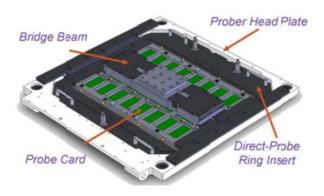


To take advantage of these process opportunities, chip designers and manufacturers seek ways to achieve the highest performance test at wafer probe. To date, manufacturers have struggled to get the test performance needed to fully perform functional testing directly on the wafer. The chief obstacle, among other factors, has been the loss in signal integrity caused by the distance between the tester pin electronics and the probe tip.

Solution Summary

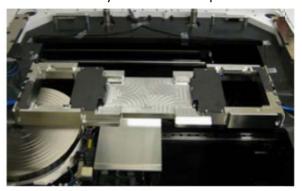
High-performance, multi-site functional testing now possible at wafer probe

The V93000 Direct-Probe solution reduces the length and number of signal path transitions between tester and probe card enabling the industry's highest test performance to now be brought to wireless, WLCSP, MPU, and GPU devices at wafer probe.



Working closely with leading probe card manufacturers, Advantest has successfully overcome traditional barriers to delivering high performance test at wafer probe. Current pogo tower-based wafer prober interfaces degrade signal quality because the signal must pass through multiple transition points and a distance of 4 to 5 inches. The Direct-Probe solution places the test head directly down into the prober and interfaces directly with the probe card. By removing the conventional mechanical interface between the wafer and tester, Direct-Probe reduces the length and number of signal-path connections between tester pin electronics and probe points, significantly improving signal integrity for device testing.

With higher quality signals, the control and performance needed for accurate simulation and full functional testing of digital, mixed-signal and RF devices directly on the wafer is possible.



Head plate with Direct-Probe kit mounted on prober

Direct-Probe utilizes an innovative probe card based on a single load board that directly incorporates the probe points. The single load board can leverage existing final test designs and can be shared between wafer probe and final test, reducing hardware development time and hardware cost.

Direct-Probe is mechanically designed and engineered for contact force management and with the planarity to support large surfaces and high pin counts at wafer test. The result: excellent mechanical and electrical contact is assured.

With the V93000 Direct Probe solution, manufacturers can now take a major step forward toward complete high performance functional testing at wafer probe and significantly lower cost of test.

Highest performance for high-volume manufacturing, multi-site probe test of digital, mixed-signal and RF devices at wafer stage

V93000 Direct-Probe's superior performance is ideal for multi-site probe test of:

 High pin count MPU/GPU devices requiring final test digital performance and high current contacting

ADVANTEST.

 Consumer audio/video, mixed-signal and RF devices that are rapidly moving to wafer-level chip scale packaging (WLCSP) and require high performance probe test

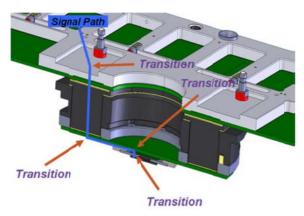
Maximum test resource utilization, high parallelism and high throughput for lowest cost of test

With greater multi-site testing (up to 32 sites based on test configuration), reduced index times (<1s) and faster test times, manufacturers can achieve the high throughput needed to drive down cost of test.

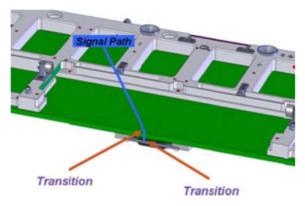
Shorter hardware development time and cost due to innovative probe card design

V93000 Direct-Probe's innovative probe card design, places the probe assembly directly on the load board, improving test performance and reducing hardware cost and hardware design time from design to production.

High-performance signal integrity from tester pin electronics to probe tip



Conventional wafer probe interface



Higher bandwidth with Direct-Probe

The current industry standard for wafer prober interface (Pogo Tower) degrades the signal quality because the signal must pass through multiple transition points and a distance of 4 to 5 inches. V93000 Direct-Probe interfaces the test head directly with the probe assembly, reducing the length and number of signal path transitions, maintaining signal integrity.



V93000 test head now fits down into prober

Mechanically designed for contact force management and planarity to support large surfaces and high pin counts at wafer test

V93000 Direct-Probe addresses all major contacting challenges (pad probe, Flip Chip, TSV and WLCSP) by supporting contact force up to 300 kg and maintaining planarity (1mil(25.4 μ m) over 44,000mm²) for excellent mechanical and electrical contact quality for large die sizes and in high pin count devices such as with MPUs and GPUs.



Features and Benefits

Scalable support of digital, mixed-signal and RF devices	Ideal for wireless, WLCSP, MPU and GPU devices; Maximum test resource utilization for greatest return on capital investment
Test head in direct contact with probe card	High-performance signal integrity for functional test at wafer stage
Multi-site (up to 32 site) capability	High parallelism and throughput to lower cost of test
Contact force up to 300KG with superior planarity	Excellent contact quality for large die and high pin count devices
Innovative probe card design	Shorter hardware design time from design to production and reduced hardware cost; Can be designed to use a single-load board for both wafer probe and final test

Related Information

For more information about the V93000 Direct-Probe Solution, please visit the following website: www.advantest.com.

Contact Information

For more information about the V93000 Direct-Probe Solution, please contact your local Advantest sales representative. **www.advantest.com**