# Tester-Per-Site® Architecture Evolution

| Generation | Test System | Electronics | Cooling | Type | Feature | I/O Pins | PPS | Benefit / New |
|---|---|---|---|---|---|---|---|---|
| 1st, 2nd<br><br>*1996* | *V1300*<br>*V3300 AD* | Individual test site controller (TSC), algorithmic pattern generator (APG), error capture ram (ECR), pin electronics and programmable power supplies (PPS) | Air Cooled | Wafer Sort | Per-Site Scalability<br>All I/O Flexibility | 512 I/O<br>10 MHz<br><br>1024<br>20 MHz | 48 | ▪ First Tester-Per-Site® (TPS) architecture for Flash memory<br>▪ More flexible in partitioning test<br>▪ Adaptive test<br>▪ TPS optimizes test time to lower Cost of Test |
| 3rd<br><br>*1999* | V4400 | Integrated TSC, APG, ECR and PPS<br><br>Electronics in test head | Water Cooled | Wafer Sort<br><br>Engineering | High parallelism for all memory devices | 2304 I/O<br>50 MHz<br><br>100 MHz in mux mode | 160 | ▪ Fully integrated Tester-Per-Site architecture<br>▪ Flash / Logic test<br>▪ 200 mm ¼ wafer test<br>▪ 36 sites<br>▪ Direct dock test head<br>▪ Optimized configurability<br>▪ Free standing manipulator |
| 4th<br><br>*2003* | V5400 | Integrated TSC, APG, ECR and PPS<br><br>Electronics in test head | Water Cooled | Wafer Sort<br><br>Engineering | 2X the number of resources - TSCs, APGs and PPS<br><br>2X the parallelism | 4608 I/O<br>100 MHz | 432 | ▪ Scalable APGs<br>▪ Dynamically configurable multi-site controller and multi-APG to match specific applications and device types<br>▪ 300 mm 1 touchdown wafer test<br>▪ 2X channels<br>▪ Flash / MCP test |
| 5th<br><br>*2005* | V5500 | Integrated TSC, APG, ECR and PPS<br><br>Matrix on top of test head | Water Cooled | Final Test | Breakthrough Matrix technology | 24,576 I/O<br>100 MHz | 384 | ▪ Single insertion MCP test<br>▪ High parallelism Flash<br>▪ Lowest Cost-of-Test for MCP |
| 6th<br><br>*2008* | V6000 series | Integrated TSC, APG, ECR, PPS, scalable frequency and performance<br><br>Electronics and Active Matrix integrated in test head | Water Cooled | Wafer Sort<br><br>Engineering<br><br>Final Test | High performance Active Matrix | 18,432 I/O<br>280 MHz<br><br>Up to 880 Mbps | 4096 | ▪ Lowest Cost-of-Test, 50% cost per pin<br>▪ 18k all I/O channels<br>▪ Scalable power supplies (PSM)<br>▪ NOR, NAND, DRAM, SRAM, MCP<br>▪ RA sub system<br>▪ Scalable performance<br>▪ Connector-less probe cards<br>▪ DRAM anti fuse repair in parallel |