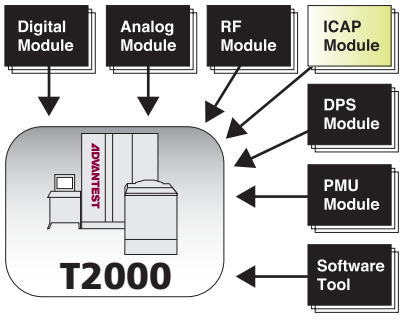
ADVANTEST

Image Capture Module

1.2Gbps CMOS Image Capture Module

This module is capable of testing the latest CMOS image sensor devices at a low cost with the embedded image capture capability that supports high-speed serial/parallel signals.



The 1.2 Gbps CMOS Image Capture ("1.2GICAP") Module is an image data capture module for the T2000 Test System designed for testing the CMOS image sensor devices.
An integrated T2000 instrument suite consisting of 1.2GICAP Module, Device Power Supply Module, Digital Module and the IP engine provides a complete test solution for CMOS Image Sensor devices.

IImage capture capability that supports high-speed differential serial/ parallel signals

- Input ports support output formats such as Sub-LVDS standard.
- Supports high-speed differential serial signals of more than 50 mV of differential amplitude sensitivity and up to 1.2 Gbps of data rate as input.
- Parallel image input consists of 16 bits of data, 1 bit of synchronizing clock and 5 bits of synchronization signal. The image data capture is triggered by the synchronization signal and stored in the capture memory.

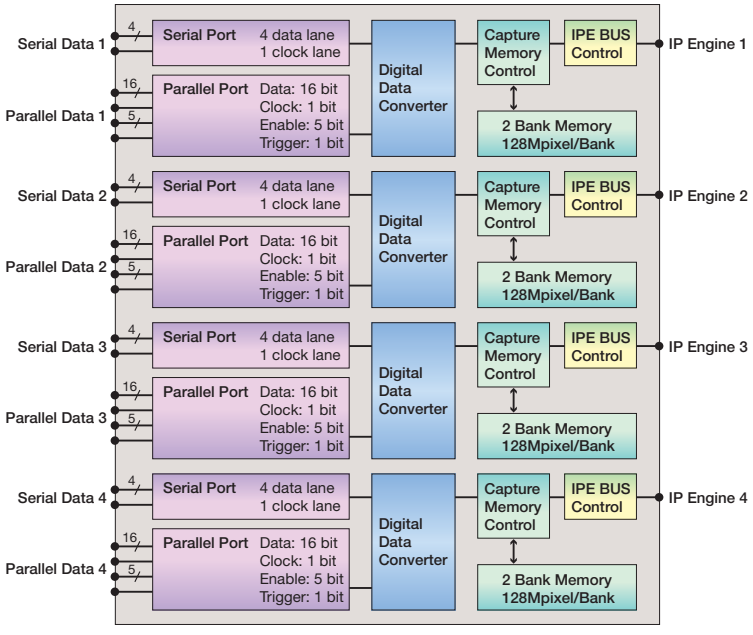
Flexible capture memory

- Capable of averaging up to a maximum of 256 image frames. Capable of detecting the low level defects.
- Continuous capture of up to 255 frames of image data. Allows evaluation/analysis of continuous images.

High throughput and lower cost of test enablers:

- Dual bank architecture enables concurrent data capture and transfer to IP Engine reducing test time Integrated PMU enables DC parametric testing without additional HW.

1.2GICAP Module Block Diagram



T2000 1.2Gbps CMOS Image Capture (1.2GICAP) Module Specifications

Serial Input	Input Lane Number (Data)		4 port x 4 channel
	Input Lane Number (Clock)		1 port x 4 channel
	Input Amplitude Range		0.05 to 2.00 Vp-p
	Data Rate		10M to 1.2Gbps
	Synchronous Data Length		64/48/40/32 bit
	Synchronous Data		SOF, EOF, SOL, EOL
	Input Clock Type		DDR/SDR/DATA STROBE
	Bit Format		RAW 8 to 16 bit
	DM Input		All pin (Interrupt via PB)
Parallel Input	Input Signal (Data, Clock, Trigger)		4 channel
			Data: 16 bit/channel
			Clock: 1 bit/channel
			Trigger: 1 bit/channel
	Input Signal (Enable)		Enable: 5 bit/channel
	Input Voltage Range		0.0 to 2.5V
	Capture Data Rate	SDR	1M to 200M pixel per second
		DDR	1M to 250M pixel per second
	DM Input		All pin (Interrupt via PB)
Capture Memory	Memory Capacity		128M pixel/bank
	Memory Bank		2 bank/channel

- Please refer to product manual for complete system specifications.
- Specifications may change without notification.

ADVANTEST®

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