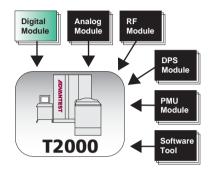
ADVANTEST

Digital Module

128ch 800Mbps Digital Module 128ch 250Mbps Capable Digital Module

A Complete 128 Channel 250/500/800 Mbps Digital Test Module for the T2000 Test System







T2000 Digital Module

- Multiple-device parallel testing is achieved with 128 I/O channels per module using high-density packaging technology.
- An optimal pattern and clock frequency that meets customer's needs can be selected by the software license.
- Each channel is equipped with a driver, comparator, DC and frequency testing functionality, as well as large capacity memory to store patterns of large size to support the ever-increasing quantity of test patterns.
- In addition to functional and DC testing, the module is equipped with standard features that allows the flexibility to test various functions such as scan pattern generator, algorithmic pattern generator, high voltage pin, multi-time domain, etc.

800Mbps Digital Module

- Supports source synchronous mode and measurement of DDR interface used by SoC devices, etc.
- A license can be selected from four frequencies, namely, 800M, 500M, 250M and 125Mbps.

250Mbps Capable Digital Module

- One histogram counter is provided per 32 channels that allows digital output data from an AD converter to accumulate in a real-time histogram for precise and efficient analysis.
- Supports multiple small-pin device simultaneous measurement to provide simultaneous measurement of up to 8 devices of 16 channels per module.
- A license can be selected from two frequencies, namely, 250M and 125Mbps.





T2000 Digital Module Specifications

Functional Test Speed Up to 125MHz in Normal Mode with 800Mbps/license: Up to 250Mbps in Double Mode Up to 400Mbps/d00MHz in Normal Mode Up to 400Mbps/d00MHz in Double Mode Up to 400Mbps/d00MHz in Double Mode Up to 105Mbps/125MHz in Normal Mode Up to 300Mbps in Quad Mode (Driver only) Timing 0 to 125Mbps/125MHz in Normal Mode Up to 125Mbps/125MHz in Normal Mode Up to 500Mbps in Quad Mode (Driver only) Timing 6 Timing Edges per Channel Timesets: 32 Local, 1024 Global 7.8125ps period and edge resolution Change period and edge resolution 150ps Edge Placement Accuracy ±200ps Edge Placement Accuracy 150ps Edge Placement Accuracy ±200ps Edge Placement Accuracy 150ps Edge Placement Accuracy ±200ps Edge Placement Accuracy 1256K Pattern List Memory 64M x 3-bits Pattern Memory per channel 4K subroutine memory per Scan Pattern Generator, per channel 16 Channel Linkable mode (26bit x 2-bits) 16 Channel 16 Channel Linkable mode (26bit x 2-bits) 16 Channel 16 Channel Linkable mode (26bit x 2-bits) 16 Channel 16 Channel Linkable mode (26bit x 2-bits) 16 Channel 16 Channel Linkable mode (26bit x 2-bits)<		128ch 250Mbps Digital Module Specifications	128ch 800Mbps Digital Module Specifications
Up to 250Mbps in Double Mode Up to 200Mbps/200MHz in Normal Mode Up to 300Mbps/200MHz in Double Mode Up to 300Mbps in Quad Mode (Driver only) with 500Mbps in Quad Mode (Driver only) Up to 125Mbps/125MHz in Normal Mode Up to 125Mbps/125MHz in Double Mode Up to 250Mbps/250MHz in Double Mode Up to 125Mbps/125MHz in Normal Mode Up to 125Mbps/125MHz in Normal Mode Up to 250Mbps /125MHz in Double Mode Up to 500Mbps in Quad Mode (Driver only) Timing 6 Timing Edges per Channel Timesets: 32 Local, 1024 Global Change triming on-the-fly capability ±200ps Edge Placement Accuracy ±150ps Edge Placement Accuracy #200ps Edge Placement Accuracy ±150ps Edge Placement Accuracy #300ps Edge Placement Accuracy ±150ps Edge Placement Accuracy #3100ps Edge Placement Accuracy ±150ps Edge Placement Accuracy #3100ps Edge Placement Accuracy 152M x 3-bits Placement Accuracy #3100ps Edge Placement Accuracy 162M x 3-bits Placemonty mode (46b #450prothmic	Digital IO Channels	128 IO channels, 8 high voltage VPP channels	128 bidirectional channels, 2 unidirectional Vpp channels
Up to 400Mbps/400MHz in Double Mode Up to 800Mbps in Quad Mode (Driver only) with 500Mbps /250MHz in Double Mode Up to 125Mbps/125MHz in Normal Mode Up to 500Mbps /250MHz in Double Mode Witiple Time Domains 200ps Edge Placement Accuracy 1200ps Edge Placement Accuracy 2100ps Edge Placement Accuracy 256K Pattern List Memory enchannel 4K Subroutine Memory per channel 4K Subroutine Memory per channel 15 Channel Linkable mode (26bit x 2-bits) 16 Channel Linkable Scan Memory mode (46b Data Fail Memory (210Aptre: 4M per channel ALPG Pa	Functional Test Speed	Up to 125MHz in Normal Mode	with 800Mbps license:
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ALPG Pattern Capture: 16M x 3 bits per pin ALPG Memory Map: 20M Central Capture Memory: 16M x 512 Pin Electronics -1.25V to +7V Drive and Compare Range -2V to +6V Drive and Compare Range -2W Resolution Termination, Load, Clamp, frequency counter per channel VPP Pins 8 per module, 13.5V maximum VIHH 2 per module, 13V maximum programmable V DC Measurement -1.25V to +6V, 32mA Maximum 6V, 25mA Maximum Central DC PMU one per Module -4V to +8V, 60mA Maximum 8V, 60mA Maximum Other Feature Histogram Engine: per each 32 channels Sequencer initiatied: source-sync margin testir Maximum ADC sample width: Single ADC: 24 bits Single ADC: 24 bits		<u> </u>	
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VPP Pins 8 per module, 13.5V maximum VIHH 2 per module, 13V maximum programmable V DC Measurement - Per Pin PMU -1.25V to +6V, 32mA Maximum 6V, 25mA Maximum Central DC PMU one per Module -4V to +8V, 60mA Maximum 8V, 60mA Maximum Other Feature Histogram Engine: per each 32 channels Sequencer initiatied: source-sync margin testin Maximum ADC sample width: Single ADC: 24 bits -			
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Central DC PMU one per Module -4V to +8V, 60mA Maximum 8V, 60mA Maximum Other Feature Histogram Engine: per each 32 channels Sequencer initiatied: source-sync margin testin Maximum ADC sample width: Single ADC: 24 bits Sequencer initiatied: source-sync margin testin	DC Measurement		
Other Feature Histogram Engine: per each 32 channels Sequencer initiatied: source-sync margin testir Maximum ADC sample width: Single ADC: 24 bits	Per Pin PMU	-1.25V to +6V, 32mA Maximum	6V, 25mA Maximum
Maximum ADC sample width: 5 Single ADC: 24 bits 5	Central DC PMU one per Module	-4V to +8V, 60mA Maximum	8V, 60mA Maximum
Single ADC: 24 bits	Other Feature	Histogram Engine: per each 32 channels	Sequencer initiatied: source-sync margin testing
Single ADC: 24 bits		Maximum ADC sample width:	
Dual ADC: 14 bits			
		Dual ADC: 14 bits	
Triple ADC: 10 bits		Triple ADC: 10 bits	
Maximum ADC Sample rate for histogram			
16 bits or less: 250Msps			
Greater than 16 bits: 25Msps			

• OPENSTAR is a registered trademark in the United States, Japan and other countries.

Please refer to product manual for complete system specifications.

• Specifications may change without notification.



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