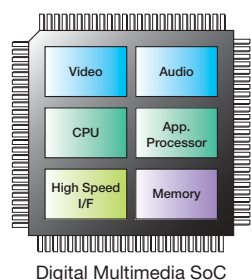


Parallel Test Solution

for Multiple Market Segments

ADVANTEST's wide-range of optimally designed modules provides flexible test solutions that can be tailored for all SoC device types.



Module Configuration Scenario

- 6.5G Digital Module
- 800M Digital Module
- AAWGD (Audio)
- BBWGD (Baseband/video)
- DPS500mA
- LCDPS

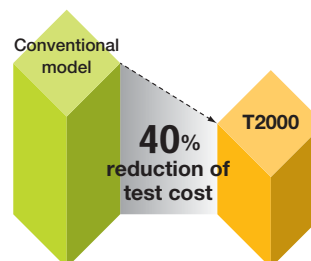


LSMF (52 slots)

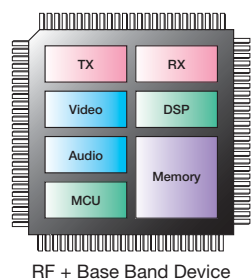
Digital Consumer Test Solution

Expandability and Flexibility

Our 52-slot LS mainframe provides the lowest test cost for the myriad of SoC devices and applications. Our modular architecture is both flexible and expandable providing customers with the lowest COT configuration for test requirement today and tomorrow. Significant improvements in parallel test efficiency afford customers a substantial test cost savings.



**Based on ADVANTEST COT model*



Module Configuration Scenario

- 250MDMA
- 12GWSGA
- DPS500mA
- AAWGD
- BBWGD

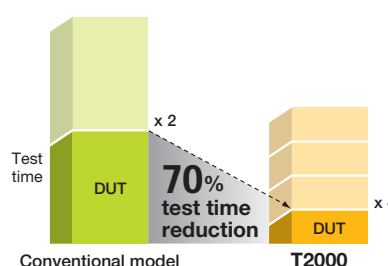


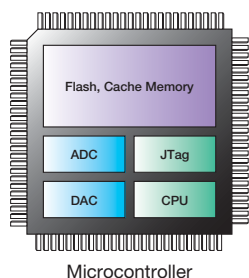
GSMF (13 slots)

RF Test Solution

Independent quad-site RF resources (32 pin, VSG/VSA) achieve unequalled levels of parallel test, and contribute significantly to a test cost reduction for volume production.

Realize 70% test time reduction per DUT with multi-site efficiencies greater than 85%





Microcontroller



LSMF (26 slots)

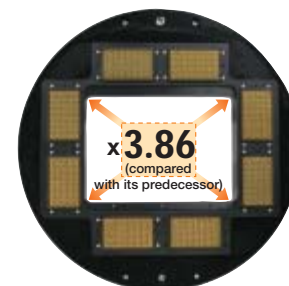
Module Configuration Scenario

- 250MDMA
- PMU32
- DPS500mA
- 2048ch Frog Unit
- Option:
- AAWGD

MCU Test Solution

Ideal coverage and broad functionality for single-pass testing of MCU devices with both embedded AD/DA, and Flash memory in a standard T2000 configuration. High-density channel resources and a newly developed pogo unit help customers achieve massively parallel testing of MCU wafer probe devices.

Increased area (178 x 253mm) and supporting more parallel testing



2048ch Frog unit

T2000-Flexible and scalable architecture addresses multiple device requirements

800MDM (800/500Mbps)

250MDMA (250Mbps)

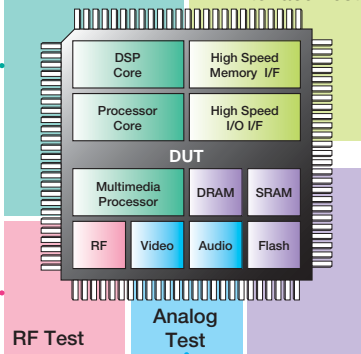
- 128 I/O pins per module
- SCAN Test Function
- Memory Test Function
- High Voltage Digital Pin
- Source Synchronous Tests (800MDM only)
- Multi Time Domain
- Histogram Engine (250MDMA only)

12GWSGA

- 4VSG/4VSA x 4MUX per module
- VSG: 6GHz, VSA: 12GHz
- High C/N Mode and High Speed Settling Mode

Digital Test

High Speed Interface Test



6.5GDM (6.5Gbps)

- Differential 8I + 8O per module
- Header Hunt Function for Non-deterministic Latency
- Clock Data Recovery for Embedded Clock Interfaces
- Clock Tracking Mode for Source Synchronous Interfaces

Device Power Supply

LCDPS

- 8ch per module
- 4A Maximum Output

HCDPS

- 4ch per module
- 16A Maximum Output

DPS500mA

- 32ch per module
- 500mA Maximum Output

PMU32 for ADC/DAC

- 32 DC pins per module
- High Speed DC Linearity Test
- Wide Coverage of Voltage Range ($\pm 0.7V$ to $\pm 40V$)
- 200mA Maximum Output

AAWGD for Audio

Audio AWG

- 8 AWG ch per module (4 L/R pair)
- 24bit/200Ksps

Audio DGT

- 8 DGT ch per module (4 L/R pair)
- 18bit/820Ksps (20bit/51Ksps)

BBWGD for BaseBand, Video

BaseBand AWG

- 8 AWG ch per module (4 I/Q pair)
- 16bit/400Msps

BaseBand DGT

- 8 DGT ch per module (4 I/Q pair)
- 16bit/128Msps
- Hardware DSP Engine

T2000 Mainframe Lineup

	SPMF	MSMF	LSMF	GSMF
# of Modules (Max)	52	52	52/26	13
MF size (WxDxH) mm	1550 x 1050 x 2000	900 x 1050 x 1900	800 x 1050 x 1600	450 x 1000 x 960
# of Site controllers (Max)	8	1	4	1
Cooling	Air/Liquid			Air

*# of modules is assumed to be only liquid-cooled modules (24mm)

- OPENSTAR is a registered trademark in the United States, Japan and other countries.
- Please refer to product manual for complete system specifications.
- Specifications may change without notification.

ADVANTEST

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