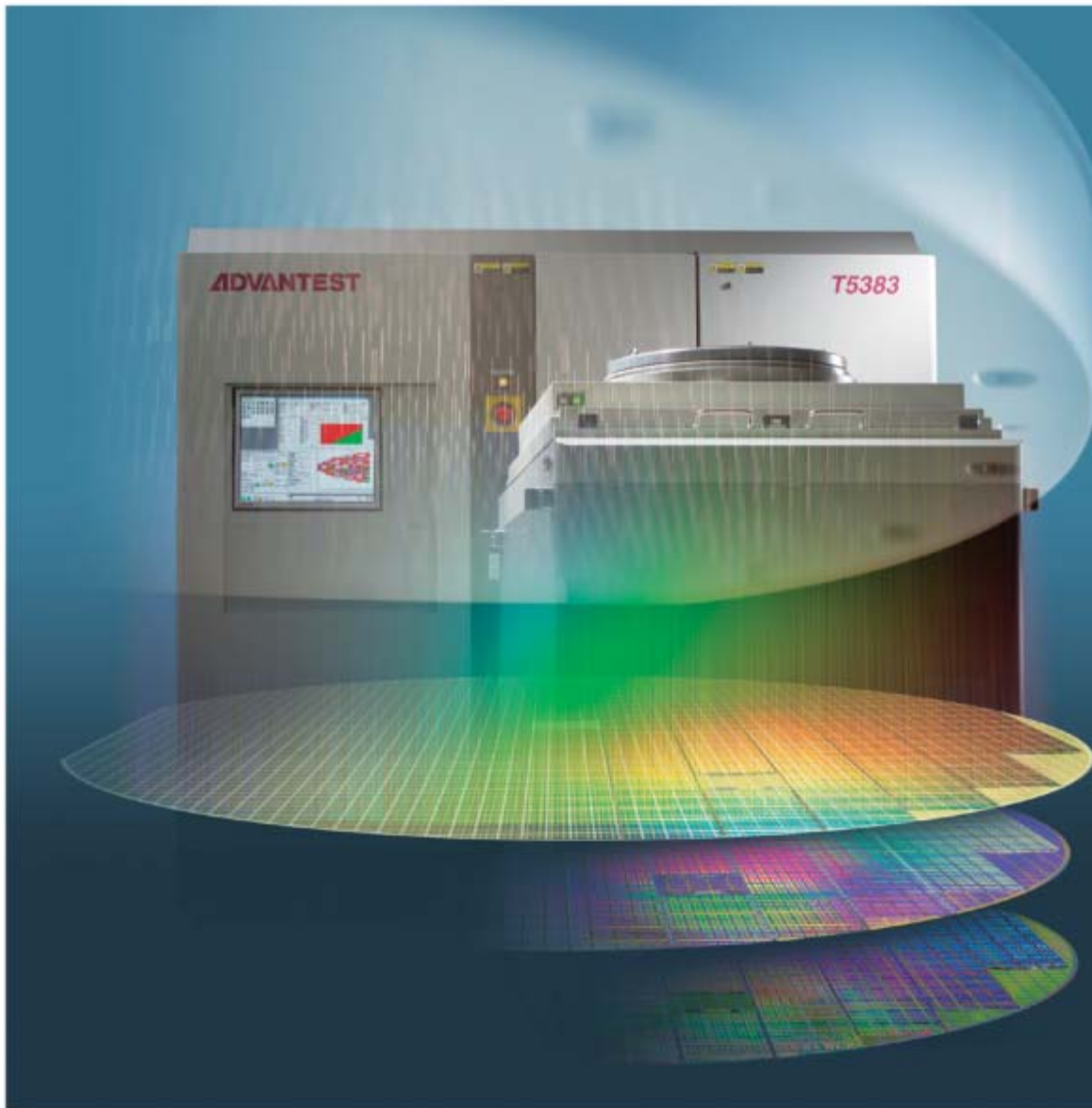


# T5383

Parallel Test for Up to 384 Devices.  
Flexible Pin Configuration Drives Lower Cost of Test.



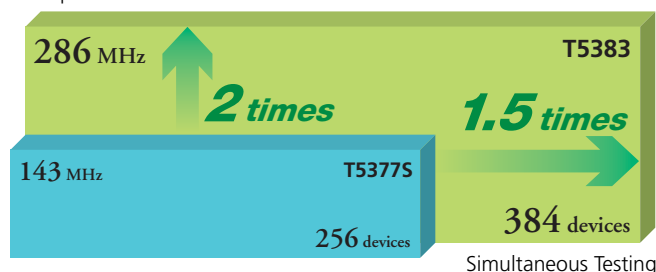
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In the DRAM manufacturing process, shrinking geometries for 300 mm wafers are taking device densities and speeds to a new level. At the same time, proliferating cellular telephones, personal computers, various digital appliances, are propelling demand for memory, particularly multi-layer SIP (System-in-Package) devices. The T5383 provides a timely response to these trends. From front-end test for DRAM to back-end test for FLASH memory, MCP/SIP, and other devices, the T5383 provides a high-throughput solution that offers flexible support for increasingly fast and versatile memory devices. In addition, T5383 high-density pin electronics deliver 50% more capacity than provided by its predecessor, T5377S, and within the same small footprint.

#### Reducing cost of test by maximizing parallel test, allowing flexible pin configurations

With greater test resources than those of the T5377S, the T5383 supports greater device pin counts, and allows for higher levels of parallelism: up to 384 devices, 1.5 times greater than that of its predecessor. Also, its flexible pin assignment capability makes possible parallel test with more flexibility and variety than ever before. This granularity of tester resources optimizes test-cell configurations, and further reduces cost of test.

Test Speed



#### Industry's Fastest Test, Shortest Test Times

The T5383 operates at 286 MHz/572 Mbps, double the speed of T5377S, making it the industry's fastest offering in this product category. This increased speed translates into shorter test times, as well as higher fault coverage, including Known Good Die applications. Further, enhanced memory repair analyzer hardware (the MRA4ev3 and DualAFM option) delivers approximately double the throughput of previous products. Faster processing speeds and dedicated high speed data communications enable production bitmap yield learning. At the same time, they prevent analysis times from increasing, even as device counts and densities grow larger.

#### Compatible with previous products

The T5383 uses FutureSuite, with its multi-language support, as its OS. FutureSuite® is compatible with the ATL language, supporting thousands of applications, and also allows programming in ADVANTEST's C-based MCI (Multi Control Interface). These capabilities enable the user to make selections tailored to evolving programming needs while leveraging existing implementations.

#### T5383 Major Specifications

Target Devices:	DRAM, SDRAM, DDR devices, SRAM and flash memory, EPROM, etc.
Simultaneous Testing:	Up to 384 devices per system
Test Speed:	286 MHz/572 Mbps (in DDR mode)



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*Please be sure to read the manual of product thoroughly before using the products. Specifications may change without notification.*

## ADVANTEST®

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