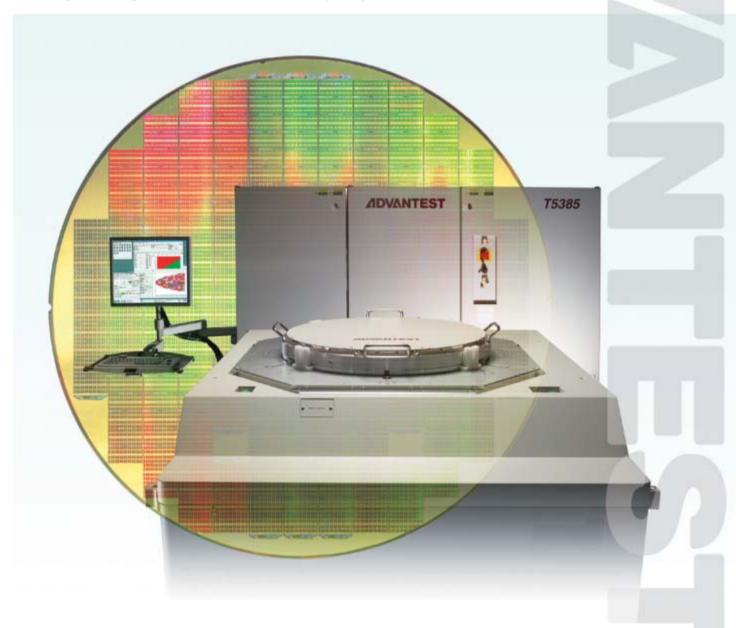


T5385/5385ES

Industry-Leading 768-DUT Parallel Test Capacity for DRAM Wafer Test



ADVANTEST's new T5385 memory test system for DRAM wafer test delivers an unrivaled 768-DUT parallel test capacity and 533 Mbps capability for increased throughput and lowered cost of test. Ideal for high-volume wafer fabs, the new tester is equipped with a flexible pin configuration that supports diverse DRAM devices, allowing tester pin resources to be optimally allocated for efficiency, reduced touchdowns and improved throughput. Achieving improved efficiency per device while scaling even higher in parallelism, the T5385 also delivers Known Good Die (KGD) for consumer devices, to greatly improve yields for LPDDR2 and DDR3 multi-die and stacked devices.

High-Throughput and Low Test Costs Achieved

DRAM memory chips used in today's computers and other electronics deliver faster processing speeds, higher data storage volumes, and more efficient power consumption than previous generation devices. To enable these gains, the semiconductor industry is aggressively migrating to smaller process nodes that allow more chips and greater densities to be produced from each wafer. Throughput has therefore become a critical issue in DRAM wafer test, with chipmakers demanding significant gains to increase productivity. ADVANTEST's new T5385 delivers an unrivaled parallel test capability and flexible pin configurations that significantly improve throughput in the wafer test process.

High-speed Memory Repair Analysis (MRA)

The T5385 is enabled by hardware and software advances, including a highspeed memory repair analysis (MRA) system for DRAM and flash memory wafer test that greatly reduces test time. In fact, test times can be shortened by 30% when compared with the company's previous model test system. Hiding redundancy processing and the transfer of yield-learning data further reduces wafer test times while improving both process parameters and business margins.

Flash-memory Capability

The T5385 also supports flash memory wafer test. It boasts a proprietary tester-per-site architecture optimized for flash memory, contributing to reduced test times.

The T5385ES Memory Test **System for DRAM Development**

Designed for engineering use, the smaller T5385ES offers all the functional and performance qualities of the T5385. Device engineering and characterization can easily be performed, and test programs developed on the T5385ES can be seamlessly transferred to the T5385, accelerating the DRAM development processes.

T5385/T5385ES Kev Specifications

Target Devices:	DRAM, SDRAM, DDR devices, SRAM, Flash memory, EPROM, etc.
Parallel Testing:	T5385: Up to 768 devices T5385ES: Up to 12 devices
Test Speed:	266 MHz/533 Mbps (in DDR mode)





T5385ES

Please refer to product manual for complete system specifications. Specifications may change without notification.

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