ADVANTEST

T5833 Memory Test System

All-in-one system supports multifunctional testing of DRAMs, NAND Flash devices, next-generation non-volatile memories and MCPs, the advanced memory technologies at the heart of mobile electronics

T5833

To keep pace with users' performance demands in the booming market for mobile electronics, the semiconductors that drive smart phones and tablet computers as well as the servers that support them – primarily DRAMs, NAND Flash memories, multi-chip packages (MCPs) and next-generation non-volatile memories including MRAM, RRAM and PCM — are becoming faster and higher capacity. This raises the need for test solutions that have both the high functionality to test today's most advanced memory ICs and the cost-efficient operation to address high-volume consumer markets.

The versatile T5833 memory test system combines industry-leading performance and low cost of test to maximize customers' return on investment. The tester is designed to perform both wafer sort and final test across a wide range of memory devices including LPDDR3-DRAMs, MCPs, high-speed NAND flash memories and next-generation non-volatile memory ICs.

High-Capacity Testing

The T5833 can achieve high throughput by simultaneously performing wafer-level testing on 2,048 devices or final package testing on 512 devices.

Known good die (KGD) testing can be conducted at speeds up to 2.4 Gbps. In addition, the tester performs high-speed failure capture and memory-redundancy analysis with AFM and MRA options, two key tasks needed for memory wafer sort. These fast functions reduce test times while enabling the recovery of more memory ICs for improved yields.

Designed for Scalability

The tester is built on ADVANTEST's modular AS Platform, making it configurable to meet each user's specific needs. The system is scalable for applications ranging from device engineering to large-volume production, and its functionality can be extended with module upgrades to handle future generations of devices.

The real-time source synchronous function increases yield and reduces test times while the T5833's tester-per-site architecture reduces test times even further for NAND and other non-volatile memory devices.

KEY SPECIFICATIONS

Devices Supported	Wafer test: All DRAMs, NAND Flash, next-generation NVMs including MRAMs, RRAMs and PCMs Package test: LPDDR3-DRAMs, NAND Flash, MCPs, next-generation NVMs including MRAMs, RRAMs and PCMs
Parallel Test Capacity	Wafer test: 1,024 (4 I/O), 2,048 (2 I/O) Package test: 512 (8 I/O)
Maximum Test Speed	2.4 Gbps
Address Fail Memory	Optional
Failure Analysis Unit	Scalable, high-performance MRA

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