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Practical design methodologies that enable concurrent testability of multiple analog and digital modules in SOC devices and provide significant reusability of ATE test vectors.

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Biography:

Jeff Brenner is a Principal Mixed Signal Test Consultant with Agilent Technologies Automated Test Group. He holds a BSEE in Electrical Engineering. He has nine years of experience in the semiconductor test industry. He has broad mixed signal test experience and consulting experience with numerous device technologies such as Audio, Wireline Communication Devices (SLIC, SLAC, xDSL), LAN, Wireless Cellular Baseband, Video and Set-top-box.

Abstract:

Recent developments in test capabilities of System on Chip (SOC) testers have extended into concurrent testability of analog and digital modules of SOC devices. Although the ability does exist on the tester, cost pressures associated with pin count on highly integrated devices can preclude the design of parallel accessibility of numerous modules. Effective planning for functional block access can enable a high degree of parallel testability. Additionally, significant advantages can be realized through the utilization of a serialized test access mechanism (TAM) optimized for concurrent access of analog modules with discreet sample clocks. Although the obvious benefit of this method of test access partitioning is to provide parallel access to multiple test blocks, we will demonstrate the concomitant benefit of reusability of developed test vectors and methods.

Introduction:

Today's SOC devices contain numerous, disparate cores. A highly evolved example of the current level of integration is a cellular baseband processor as shown in Figure 1.

A basic premise of testability of an analog core is direct access. Commonly, digital test accessibility is provided through a combination of memory I/O pads and multifunction pads to enable SCAN. For the analog cores, the analog interface is externally available due to the operational requirements of these devices. But, as direct data

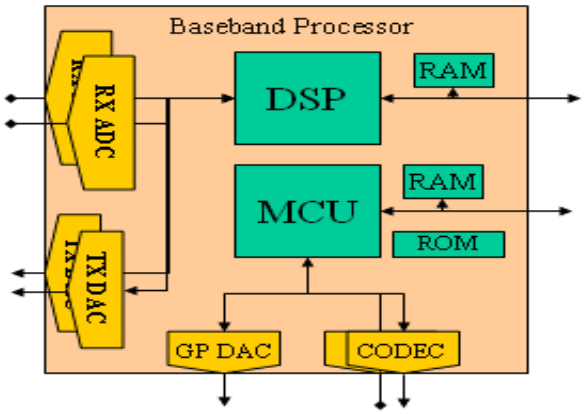

Figure 1: Baseband Processor Block Diagram

I/O external access of the analog cores is not required for operational functionality it is often not added for testability. In many cases, the Design For Test (DFT) methodologies are implemented as test modes with test module communication through the digital core that operationally communicates with the analog core, such as a DSP. Although this provides test access, it precludes concurrent testability of the analog module and the digital module that is communicating with it during test. In historical ATE architectures, the cost of test (COT) impact

was minimal since these systems tested the cores of an SOC device sequentially.

Today's per-pin ATE architectures provide significant concurrent test capability, of both digital and analog cores, which can be scaled to match the parallel accessibility of the cores under test. Implementing optimized design for concurrent testability provides an opportunity to decrease the overall test time while providing improved test coverage over sequential test. This has created a cost justification for the necessary design process changes. The concurrent operation of the cores provides a test coverage capability which best simulates the final system mode operation of the device. This may provide coverage for test escapes which may not otherwise be identifiable on ATE systems.

Mixed Signal Concurrent Test Defined:

Concurrent test has been enabled through the fundamental architectural changes of ATE systems. In the 1980's, ATE systems were developed around a single, master sequencer. This sequencer was responsible for controlling the timing and synchronization of all the digital and analog resources. In the 1990's, a new architecture was developed which was based on a per-pin sequencer. A digital ASIC at each tester pin provides all of the sequencer control necessary for that pin. This allowed asynchronous operations on groups of pins, referred to as ports[1].

Digital concurrent test is the ability to segment the tester resources into multiple ports with disparate digital test functionality operating concurrently on each port at different operational frequencies. The example baseband processor SOC contains an MCU core, DSP core and memory. The test of these cores may require that different SCAN chains are executed on each processor core while an APG test is executed on the memory. Historic test methodologies would have multiple test modes which would test each of these cores sequentially. The master sequencer would first change to SCAN mode to execute the test at Frequency 1 on the MCU core, then change the master clock frequency and execute the SCAN test on the DSP core, then again change the master frequency and the operating mode to Memory Algorithmic Pattern Generator (APG) to test the memory core. All operations occur sequentially. In a digital concurrent test implementation, all defined ports would be set to the necessary operating frequency and mode in parallel, followed by parallel execution of the core tests (Figure 2). The throughput benefit is derived from the savings in both test execution and setup times.

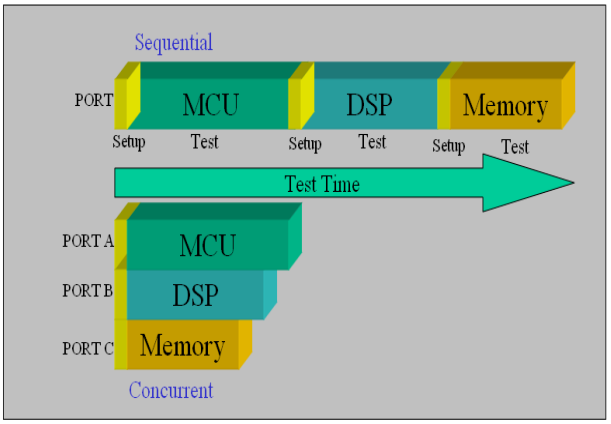

Figure 2: Concurrent Throughput Impact

Mixed signal concurrent test requirements go beyond those of digital concurrent test. There are several additional functional requirements for testing the analog modules. These include: digital capture, arbitrary waveform generators (AWG) and waveform digitizers (DGT). As in the case of the test vector generators, for true concurrent test capability, each of these tester resources must have autonomous capability.

Digital capture is the ability of the ATE system to capture the drive state of the digital outputs of the device under test. This is necessary for capturing the resultant data from an analog to digital converter (ADC) module. Concurrent test capability requires that the capture capability is available on a per-pin basis allowing independent digital capture ports to be defined on the granularity of a single pin.

In order to have true autonomous concurrent testability of ADC cores, it is necessary to provide an AWG with autonomous sequencing coinciding with the digital test port that captures the ADC core data. Conversely, for digital to

analog converter (DAC) core testing, a waveform digitizer with similar sequencing capabilities is necessary. The AWG and DGT must also have the ability to be clocked independently of the digital module under test to maintain coherency for FFT analysis[2].

Design for Concurrent Test Access:

Today, IEEE 1149.4 is an existing standard relating to DFT of analog cores. The standard is primarily designed for test access to an internal analog node within an SOC device. It does not adequately address the digital interface of analog cores[3]. Internal analog cores are designed to directly interface to the associated digital control block (Figure 3). A standard TAM would provide a shared access port which could only address the analog cores sequentially.

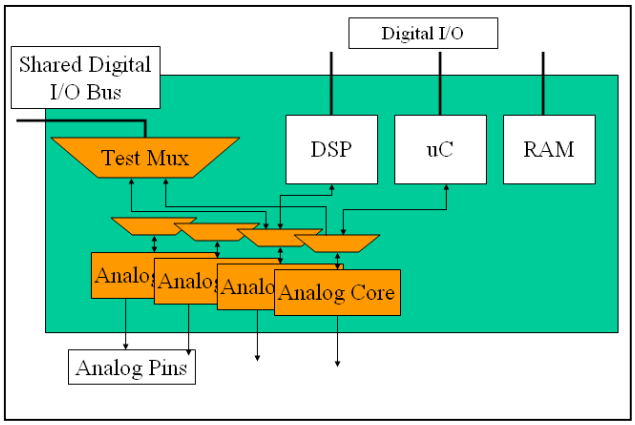

Figure 3: Non-Optimized Shared TAM

In reduced pin count design for concurrent test (RPC DFCCT), this same interface is developed using an individual Test Access Port (TAP) for each analog core to enable full parallel accessibility (Figure 4). The three pins which compose this TAP are the Analog Test Data Input (ATDI), Analog Test Clock (ATCLK), and Frame Clock (FCLK). The ATDI pin is the serialized source waveform data. The ATCLK provides the clock for the shift register. FCLK is used both for latching the data from the shift register and as a conversion clock for the DAC module.

The TAP for an ADC core is functionally similar to that for a DAC. In the case of the ADC, ATDI is now Analog Test Data Out (ATDO). In order to maintain synchronous data sampling between the analog module and tester, ATCLK is driven by the tester.

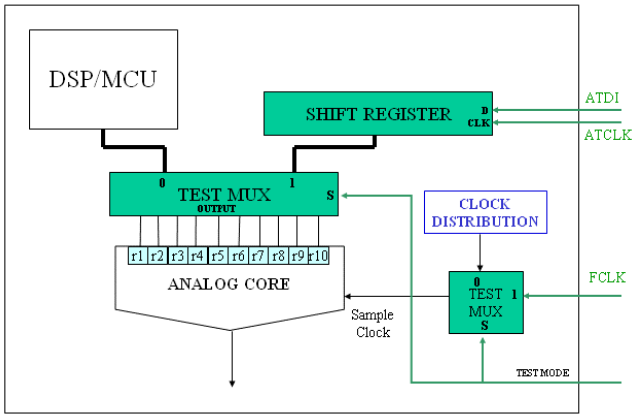

Figure 4: Per-Core TAM

Consideration must also be taken of the package I/O bandwidth when implementing these design changes. The requirements are determined simply by multiplying the number of data bits per word by the effective sample rate of the analog core. For example, a cellular baseband device may incorporate a 10 megasample 12 bit DAC. The serial data bandwidth is simple 12 bit x 10 Mega sample MSPS, or 120 Mbps (Mega bit per second). This is a readily available bandwidth in most cellular baseband packages.

In marginal conditions, where the available package bandwidth would not support full serialization of the output, a modified design can be implemented. As an example, if you have a package with an I/O bandwidth limited to 100Mbps, and a DAC which is 10 bit at 20MSPS (200Mbps), you can modify the serialization logic and test pin count to meet your need. In this case, simply changing the number of test data pins to two and modifying the serialization logic will meet the device test needs.

Some devices require significantly higher converter rates, on the order of several hundred MHz at 10 bits. It is not reasonable to serialize this data. In this instance a parallel port should be incorporated to insure testability by the ATE system.

A RPC DFCCT implementation of the analog cores in the baseband processor, as described in Figure 1, would require only fifteen test pins. As each I/Q and CODEC converter pair can share sample clocks, the seven cores require seven test data pins, four test data clock pins and four frame clocks.

Vector Reuse:

The components of a single test in a test flow are: test vectors, digital and analog waveform segments and the test method. The test method is a customizable program block used to setup ATE resources and analyze the result data.

An individual test vector is generally composed of two parts. The first part programs the device under test in order to put it into the proper mode of operation, such as a test mode which enables proper access to the cores under test. The second part of the test vectors is the actual test stimulus, generating the source and comparing the results for the cores being tested. This test stimulus can be digital functional vectors, structural test vectors or digital waveform vectors for DACs. As historical architectures provided only one effective port, each test vector defined all device pins to operate at the frequency and within the mode of operation for that test.

In concurrent test vector generation, the test vectors can be split into ports to match their functionality. Ports can be defined and re-defined dynamically through the course of execution of the test flow. This allows the segmentation of the test mode setup vectors separately from the test stimulus vectors and further segmentation of each core (Figure 5).

A multi-port based approach can provide significant development time savings in the initial test development process. The test of an individual core using the single port vector generation process includes simulation of both the test mode setup and stimulus, which is then converted to test vectors. This entire process must be repeated for every test in the flow. A multi-port approach to vector generation requires that the test mode setup simulation is created one time. It is then re-used with all the corresponding test stimulus vectors.

It is common for SOC devices to undergo numerous incremental design changes of individual cores over the product lifetime. Incremental design changes made in the device often require a change in the test vectors to enable the proper test mode. This change in a single port architecture necessitated the regeneration of the entire test vector, test mode setup and test stimulus. In multiport, concurrent test vectors, when a generational design change is created, the only change required is to the setup vector. The stimulus vectors can remain the same if the core they address has not changed. Likewise, if an individual core is modified, it necessitates only the modification of the vectors for the relevant port.

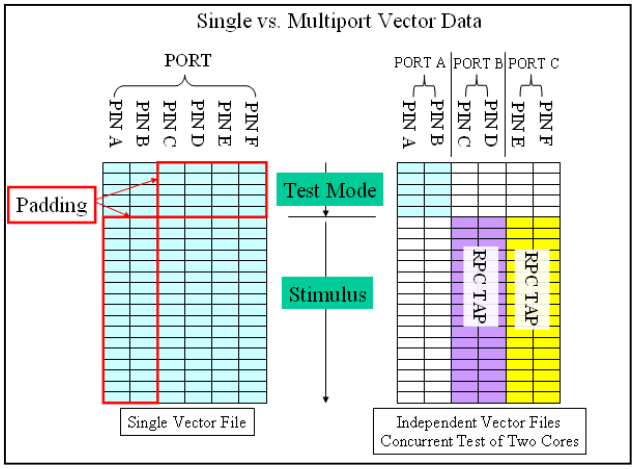

Figure 5: Multiport-Based Test Vector Segmentation

The debug process is also significantly streamlined with DFCCT implementation. As single port vectors contain multiple time domain sections to cover the setup and stimulus components of test, troubleshooting is often complex. Concurrent test multiport vectors allow focus on the specific functional block at the native device cycle frequency.

This per-port vector capability now enables the ability to create ATE IP test libraries which can be carried forward and reused as are the IP blocks

within an SOC. These IP test libraries contain the port vector file, analog stimulus file and test method.

Cost of Test Benefit:

SEMI E35 demonstrates a linear relationship between the throughput and cost[5].

$$COO = \frac{FC + RC + YC}{L \times TPT \times Y \times U}$$

where:

COO = Cost per good unit
FC = Fixed Cost
RC = Recurring Cost
YC = Cost of Yield Loss
L = Equipment Life
TPT = Throughput Rate
Y = Yield
U = Utilization

The implementation of parallel TAMs impacts throughput by enabling concurrent testability of cores. Recurring costs are reduced through test vector reusability.

Conclusion:

Implementations of concurrent test solutions have demonstrated test times reductions of over 30% while demonstrating results which correlate to sequential test methodologies[6]. The design methodology presented demonstrates an alternative method for optimizing the parallelism of test access to analog cores while minimizing the impact to device pin count, which is a significant component of device packaging cost. Although COT reductions alone justify this approach, the additional beneficial impact on test vector reusability can provide significant time to market benefits.

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