Parallel RF Wafer Sort Production Testing

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Abstract
The increasing demand for smaller, thinner and more complex portable electronic devices is driving the chip package to incorporate multi-die and wafer-level packaging. A key benefit for multi-die packaging is that dies from different manufacturers or fabrication processes can be incorporated without taking up too much space. Wafer-level packaging has the advantage of allowing very thin chip packages, demanded by razor thin electronic appliances and super-compact consumer products. However, both types of packaging inherently require that the dies be tested at wafer level.

RF wafer sort testing poses unique challenges with requirements for high signal integrity at high frequencies and bandwidth. This paper will discuss the measurement challenges and considerations for known good die testing of an RF SOC (system on chip) device. It will explore the challenges of setting up the multi-site wafer probe card and assembly. It will then discuss factors taken into account when selecting a probe station, RF wafer probe card, and ATE (automatic test equipment) test system. Challenges of testing RF performance on-wafer are described.

Key Words – Parallel RF Wafer Sort, Prober, RF Probe Card, ATE

1. Introduction
Several years ago, RF wafer sort was done single site. DC screening was done at wafer sort and full functional and RF test was at package level. As a result, there was only limited ability to reduce overall test costs of a device. Also the customer need for KGD (known good die) delivery could not be meet. KGD is a requirement to allow fast and cost effective process and technology feedback. It is necessary, if SIP (system in package) or MCM (multi chip module) technology is used, because package scrap can be reduced with this method.

What has changed since then? RF probes are available that allow full parallel at-speed test at wafer level. Even complex RF tests like BER (bit error rate) or EVM (error vector magnitude) are done fully in parallel. This significantly reduces overall test costs of a device and helps to meet the KGD requirements.

The reasons for this change are on the customer, vendor and technology side. On the customer side, there is a high pressure to reduce costs. PRFWS (parallel RF wafer sort) helps to reduce the increased costs of package scrap. In addition, it helps to meet the KGD need for CSP (chip scale package), MCM, or flip-chip assemblies. On the vendor and technology side, major improvements in SOC integration – e.g. implementing RF functionality in CMOS technology – made PRFWS necessary. In addition, probing at high frequencies as well as ATE with high parallel SOC and RF functionality are available and interesting from an economical point of view.

2. ATE Test Challenges

In general, there is a need for high throughput, high parallel efficiency and high RF port count – all requiring a higher level of integration. In addition, since all kinds of RF tests can be performed like EVM, ACLR (adjacent channel leakage ratio) or BER, there is a need for a wide bandwidth and a large instantaneous dynamic range.

Not only CW (continuous wave) RF tests are done on wafer level, but all types of modulated tests that require wide bandwidth performance. In general, consumer and industry are requesting higher data rates. One way to achieve this is with a wider bandwidth. As a consequence, the new standards are increasing their channel bandwidth as the 40MHz bandwidth example of the WLAN standard 802.11n is showing in Figure 1.

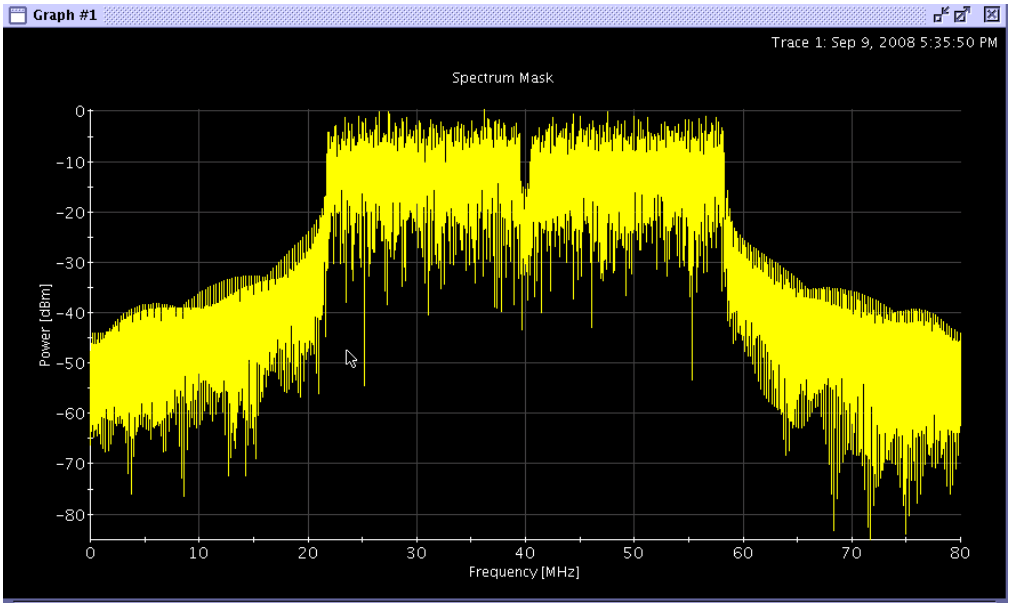

Figure 1. 40MHz bandwidth of WLAN 802.11n standard.

Another possibility to improve performance and data rate is to increase the dynamic range. The two important terms in that context are Spurious Free Dynamic Range – the ratio of the maximum power and the biggest spur – and Instantaneous Dynamic Range – the ratio of maximum power and the power of the noise floor (Figure 2). These terms are critical for measuring small signals in the presence of large signals, such as noise figure, ACLR, TOI (third order intercept point) and phase noise measurements. Large dynamic range results in better accuracy and less averaging, ultimately providing higher throughput.

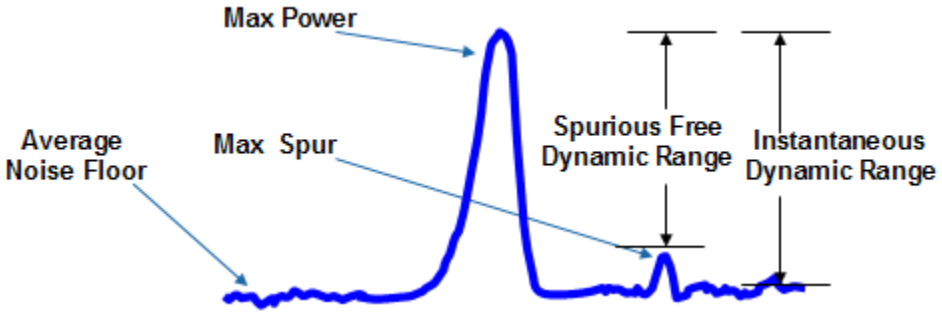

Figure 2. Definition of Spurious Free and Instantaneous Dynamic Range.

Since the trend goes to full function test at wafer level including RF, the ATE must incorporate sufficient RF ports also for wafer test mainly due to three reasons:

1. Higher integration of different RF standards like WLAN, GPS, Bluetooth, multi-band cellular into one silicon (as for the next generation of RF super cellular chips) require more RF ports.
2. New RF technologies like MIMO (multiple input, multiple output) that help to improve communication contain a couple of antennas.
3. And finally multi-site testing simply doubles or quadruples the port count for dual or quad site testing.

The key ATE requirement for PRFWS testing is sufficient RF ports with plenty baseband and digital resources that enable full parallel RF source and measure. To take advantage of the parallel test capabilities a high parallel efficiency is necessary together with the capability of wideband testing with sufficient instantaneous dynamic range.

3. Prober

RF probes need cleaning from time to time at least as often as probes for any other application. Therefore, cleaning speed is an important consideration. Other important considerations - especially for RF - are temperature control and shielding for a low-noise environment. Further topics are the index time (time chuck requires to move from one die to the next), the step size resolution (for multi-site see section 4), the degree of wafer alignment, calibration, ease of use and speed of reconfiguring the probe card station. For most outsourced projects the available prober is determined by the OSAT (outsourced assembly and test) companies and is not selectable.

4. Probe Card and Assembly

More influence can be taken by selecting the right probe card. Key requirements are sufficient frequency bandwidth, port match and number of test points on the die (probes). Further consideration is regarding the available variety of probe assemblies. Each technology has its advantages and disadvantages. We will highlight the key aspects of Cantilever, Vertical and Membrane probe (Figure 3) [3][6].

Figure 3. From left to right: Cantilever, Vertical and Membrane Probe (courtesy of Cascade Microtech Inc.).

For Cantilever probes, parallelism depends on the pad layout – over 2000 probes are possible. Due to possible crossing of the probes, the array pad layout is most challenging; in-line is best for parallelism. Typically, the maximum bandwidth is 400MHz. However, there are RF Cantilever Probes – e.g. twisted probe pairs – that allow better performance up to 3GHz.

Vertical Probes allow very high parallelism with over 5000 probes possible, but with higher pitch and higher costs. Standard vertical probes are not appropriate for RF. However, there are vertical RF probes available for up to 5GHz.

Membrane probes provide the best RF performance with up to 20GHz. The available second generation of membrane probes enable sufficient parallelism with up to 800 probes. They have a very long lifespan, but at higher cost, which is especially true for multisite applications.

Also the pad layout of the die needs to be considered. The contact pads can be arranged differently: The pads can be located at the perimeter, in-line or as an array. Each pad layout matches differently with the different probe types. The colors in Figure 4 provide a first direction (green means appropriate, red not appropriate). Membrane technology typically matches with the different pad layout arrangements, if the number of probes is not too high.

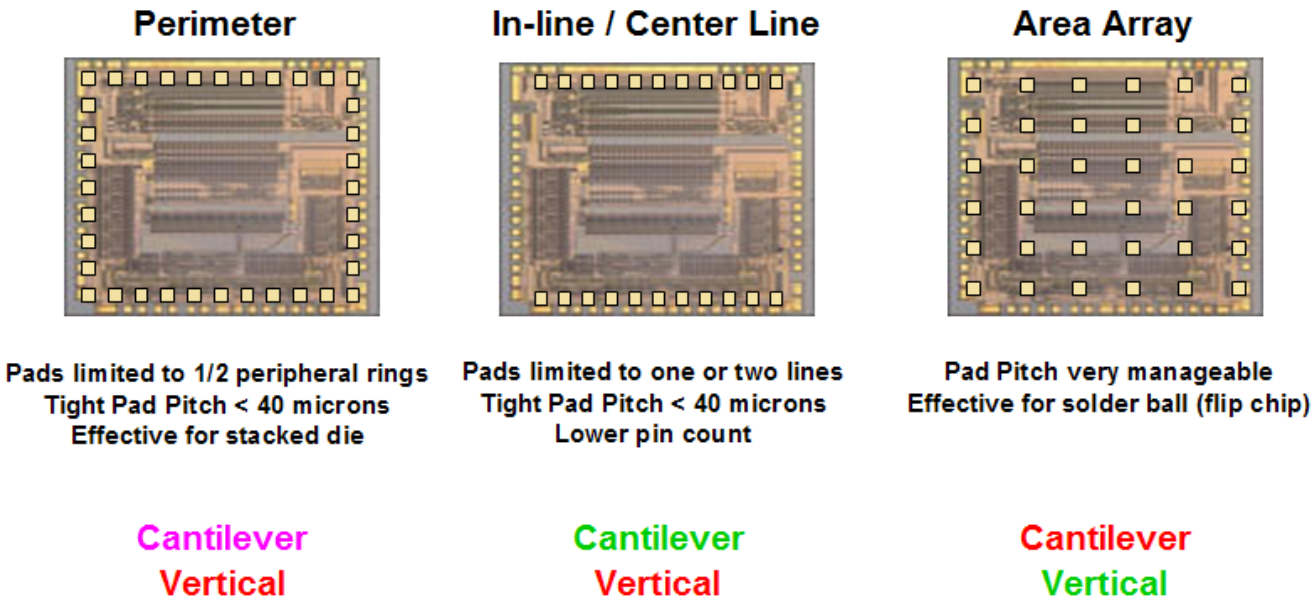

Figure 4. Die pad layout considerations for different probe types.

The wafer probe structure must not only match the die pad layout and pitch. To make good contact to the wafer, the probe core must handle planarity adjustment and compliance. The isolation of RF signals from any other signal to avoid crosstalk is critical for RF probing. Other considerations are impedance control to minimize reflections, the ability to install decoupling capacitors on the probe core or at least close to the DUT (device under test) to reduce noise and other supporting circuits required for the DUT to operate correctly.

Figure 5 shows the picture of a membrane probe from Cascade called “pyramid probe”. The term *pyramid* comes from the plunger in the center that gives the probe the shape, but also the right alignment and force towards the wafer. The needles are arranged at the top (see zoomed picture at upper right in Figure 5). This type of probe features 50 ohm traces, the possibility to place tuning circuits close to the needles, low parasitic inductance and therefore excellent RF performance. We measured a 3dB bandwidth of 20GHz (lower right picture in Figure 5).

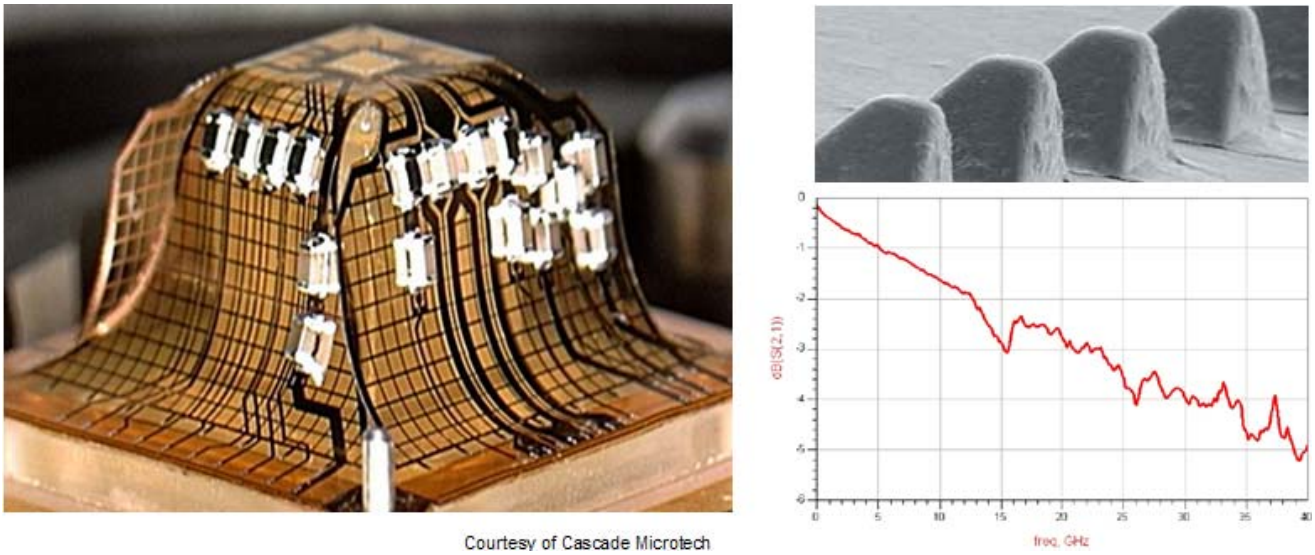

Figure 5. Example of membrane probe with tuning circuitry, zoomed needles (courtesy of Cascade Microtech Inc.) and bandwidth.

The probe assembly connects the wafer probe, the probe card and the DUT board with the probe card mounting ring with the tester. The key requirement for good RF probe assembly is excellent signal path integrity, while a large number of RF ports are handled. It needs to be easily set up to not incidentally break any RF connections in the production environment. It also should allow debug with external connections and of course ensure good isolation between sites for signal integrity and repeatable measurements.

How can signal integrity be ensured in PRFWS? Here just a few rules of thumb. The first generic recommendation is to minimize the number of hardware components on the DUT board and probe card. This will reduce the potential risk for crosstalk, mismatch and downtime due to broken DUT or probe card. Also the need for additional RF calibration of the external components does not exist. The idea is to let the RF tester do the whole job. Another important point is the correct signal trace impedance of the RF lines. This ensures minimal reflections at maximum power transfer. Typically, the return loss should be -14dB or less. Last, but not least, the PCB layout needs to be done properly. Low-level signal tests require minimal crosstalk between traces. This can be ensured by separating the different types of signal traces, isolation with ground planes and placing different types of signals like digital and RF on separate DUT board layers. Of course, an easy docking interface between the probe assembly and the tester is important. This speeds up parts changeover and reduces the risk that the probe card gets damaged.

Figure 6 shows the current implementation for a Verigy probe assembly. Bottom side connects the tester; top side the wafer. Main elements are SMP type RF connectors at the test head and tester pogo pins to connect DC, digital and analog with the DUT board. On top of the DUT board, there is another pogo tower that connects to the probe card. The RF signal is connected using another coaxial cable for RF signal integrity and easy debug access.

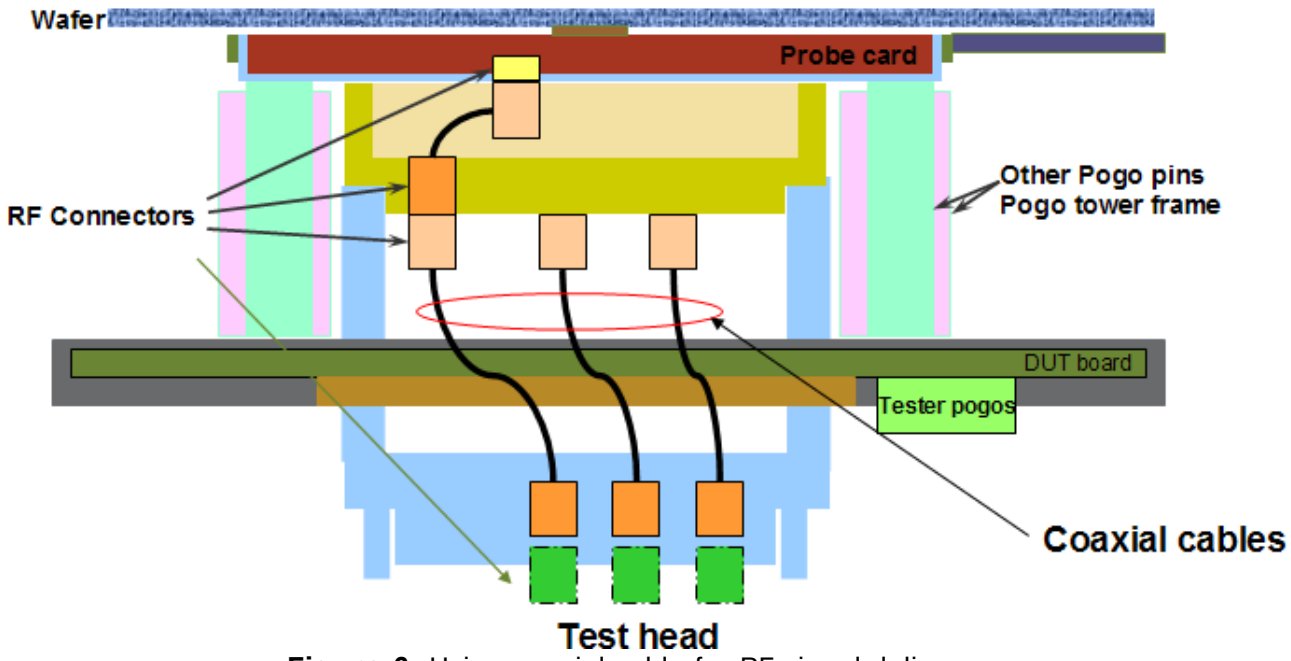

Figure 6. Using coaxial cable for RF signal delivery provides signal integrity and debug access.

5. RF Calibration

There are several RF calibration options for wafer probing. We will discuss the three most common approaches. Option one represents the optimum case regarding RF performance. Here, calibration is done with "wafer reference standards" at the wafer probe tip using special structures on the wafer serving as open, short, load and through. Since this requires additional hardware and more complex calibration steps, it is typically used only in a characterization environment.

More common is option two. First of all, calibration is performed for the tester RF ports using ATE equipment. De-embedding can be achieved if the probe's S-parameter data file, which is provided by most manufacturers, is mathematically concatenated with the tester calibration data. Advantage is that this approach corrects both magnitude and phase information. This is a good choice, because the tester calibration is fast and simple and the EM models of the probe assembly have improved a lot.

Option three is also common. As for option two, the tester RF ports are calibrated with ATE equipment. However, here the insertion loss offset of the wafer probe assembly is measured with the bidirectional couplers of the RF instrument. Disadvantage of this approach is that it corrects only magnitude information. However, this is certainly enough for RF projects performing just CW measurements. Overall, option three is a good and simple approach that is suitable for high volume manufacturing.

The overall RF performance is always limited by its weakest link in the whole signal path. Therefore, the whole probe configuration needs a proper setup. This includes a simple and controlled impedance interface, simple DUT board and probe card design, minimizing crosstalk and reflections, proper RF calibration and ATE with stable and repeatable measurement capabilities.

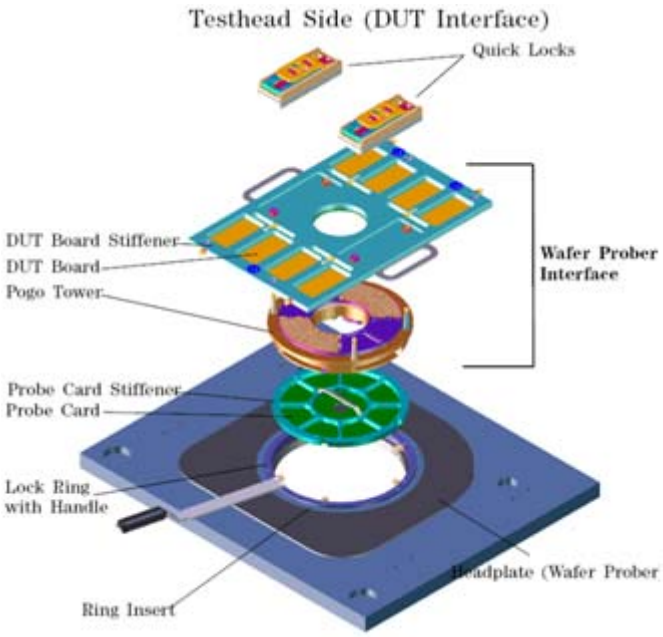

Figure 7. Example of a typical Verigy RF Probe Setup.

6. Conclusion

Probe technology and ATE SOC and RF implementations provide today a proven RF wafer test solution for multisite. This includes ATE RF requirements discussed earlier in the article as well as other, mandatory SOC test requirements like enough digital pins, power supplies and digital and analog performance. RF performance is proven in terms of cross-talk and measurement repeatability. Currently, dual-site test is common for RF wafer sort, but there are also quad-site (and more) projects on the way.

Parallel RF wafer sort production testing is possible and has become a common essential in the industry. However, an on-wafer test project can only be implemented successfully, if all of the important factors are taken into consideration:

- Understanding ATE Test requirements,
- Prober selection,
- Wafer probe assembly designed to maintain signal integrity,
- RF calibration to provide accurate results.

7. References

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