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16 Gbps 4-PAM Signal Comparison for Real-Time Testing of Multi-Level Signal Transmitters

Masahiro Ishida
Advantest Corporation

Abstract

This article proposes a method for testing a device with multi-level signal interfaces. This method utilizes multi-level comparators that are based on a new concept. The multi-level comparators realize real-time functional testing of a multi-level signal with the same number of comparators as a conventional test system, by changing the threshold voltage levels dynamically in response to the expected values of a signal under test. This dynamic threshold comparator concept is suitable for a system testing a high-speed multi-level signal. This method is also scalable for an increase in the number of voltage levels such as 8-PAM and 16-PAM signals. Experimental results are discussed with a prototype circuit that demonstrates the proposed concept applied to a 16 Gbps 4-PAM Test System.

1. Introduction

Recently, many studies of the multi-level signal transmission method such as pulse amplitude modulation (PAM) technique have been published [1, 2], and all of them shows that the PAM interfaces are promised techniques for improving the transmission rate. Currently, PAM is mainly applied to long-distance transmissions such as Ethernet. However, we believe that with the demand for a higher-speed transmission rate, the PAM technique will be expanded for short distance transmissions such as inter-module and chip-to-chip transmissions.

In order to put the multi-level signal interfaces to practical use for mass production, cost reduction of the multi-level signal interfaces is essential. This means that a cost reduction for testing is also indispensable.

A conventional multi-level signal testing method samples the multi-level signal under test with an A/D converter and analyzes the sampled waveform by digital signal processing (DSP) techniques afterward. For example, the compliance test of Ethernet [3] provides an analysis method of a transmitter output signal waveform by using a high-speed digital real-time oscilloscope. Such a DSP analysis method has a problem in that the analysis time is very long. Consequently, the conventional method can be applied only to devices with smaller number of interfaces, but cannot be applied to devices with a great number of interfaces.

On the other hand, ATE vendors supply digital modules for testing high-speed serial interfaces in real-time. Even though, many studies of high-speed interface testing methods have been conducted [4-6], these methods are developed only for testing binary signal. No real-time testing solution for the multi-level signals has been released at this time.

Our mission is to develop a low-cost testing solution for the multi-level signal interfaces that will be available in advance of anticipated need for mass production. In this article, we propose a real-time functional testing technique for multi-level signal interfaces, especially multi-level signal comparison technique for testing transmitter devices.

The rest of the article is organized as follows. Section 2 describes the multi-level signal transmitter testing and the conventional test system. Section 3 presents a concept of the proposed test system. Section 4 provides experimental results with a prototype circuit to demonstrate the proposed concept. In Section 5, the other applications of the proposed method are discussed. Finally, Section 6 summarizes the article.

2. Multi-Level Signal Transmitter Testing and the Conventional Test System

2.1 Challenges for Testing Multi-Level Signal Transmitter

Table 1 shows test items for transmitter (Tx) devices. In the production test of Tx devices, it is essential to test the voltage variation (voltage noise) and the time variation (jitter) in the output signals from the Tx device against specified limits. Hence, output voltage margin testing and jitter generation testing are particularly important among all those test items.

Table 1: Test Items for Transmitter Devices.

Test Item	Description	Priority in Production Test
Functional Testing	Testing the functionality of the DUT	High
Output Voltage Margin Testing	Testing the output voltage levels to be within the predetermined range	High
Jitter Generation Testing	Testing the output jitter to be within the predetermined range	High
Eye Margin (Eye Mask) Testing	Testing the eye openings to be larger than the predetermined eye mask	Middle
Emphasis (Equalizer) Testing	Testing the emphasis levels to be within the predetermined range	Middle
tr/tf Measurement	Measuring the rise and fall times of the output signals	Middle
Output Jitter Measurement	Measuring the timing jitters of the output signals	Middle
Skew Measurement	Measuring the timing skews between the output signals	Middle
DCD Measurement	Measuring the duty cycle distortion levels of the output signals	Middle
Output Voltage Level Meas.	Measuring the output voltage levels	Low
Common Mode Voltage Meas.	Measuring the common mode voltage levels of the output differential signals	Low
Eye Diagram Measurement	Measuring the eye opening diagrams of the output signals	Low
SSC Measurement	Measuring the quality of the spread spectrum clocks	Low
Overshoot/Undershoot Meas.	Measuring the overshoots and undershoots of the output signals	Low
Output Impedance Measurement	Measuring the output impedances of the output drivers	Low

Output Voltage Margin Testing: This confirms that the voltage level of the Tx output signal is within a specified range. For the voltage margin testing of the multi-level Tx devices, a dual-threshold comparator is required.

In the case of a binary signal, in order to test the voltage margin of Tx output signal, it is confirmed that the output High voltage level V_{OH} is higher than its lower limit value $V_{OH,min}$ and the output Low voltage level V_{OL} is lower than its upper limit $V_{OL,max}$ at the predetermined strobe time T_{STRB} (Figure 1(a)). The voltage margin testing of the multi-level signal also confirms that each voltage level V_{Ok} of the Tx output signal is within each specified range ($V_{Ok,min}$ to $V_{Ok,max}$). Therefore, for each voltage level V_{Ok}, it is required to compare the output voltage with both the upper limit $V_{Ok,max}$ and lower limit $V_{Ok,min}$ of its expected value simultaneously at the predetermined strobe time T_{STRB}. Therefore, a dual-threshold comparator is needed for the output voltage margin testing of a multi-level signal (Figure 1(b)).

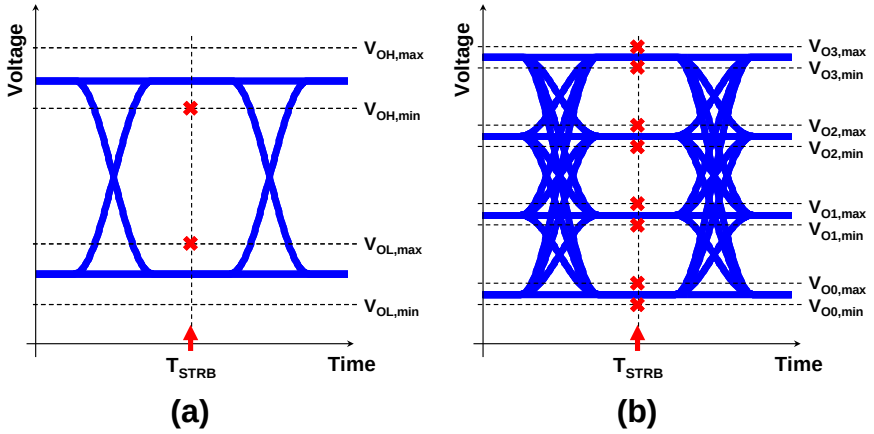

Figure 1: Output Voltage Margin Testing of the Tx Device. (a) Binary Signal. (b) Multi-level Signal.

Jitter Generation Testing: This confirms that the transient time deviation of the Tx output signal is within a specified range (allowable jitter). For the jitter generation testing of the multi-level Tx devices, the existing high-precision timing generator [7, 8] used for testing binary signals can be applied.

The jitter generation testing of a binary signal confirms that there is no bit error at the predetermined times (T_{STRB1} and T_{STRB2}) of the signal under test (Figure 2(a)). In the jitter generation testing of a multi-level signal, we may set the strobe time at both ends of the eye of the signal under test just like for the binary signal (Figure 2(b)). Therefore the jitter generation testing of the multi-level Tx devices using the multi-level comparator can be realized by using the high-precision timing generator already developed [7, 8].

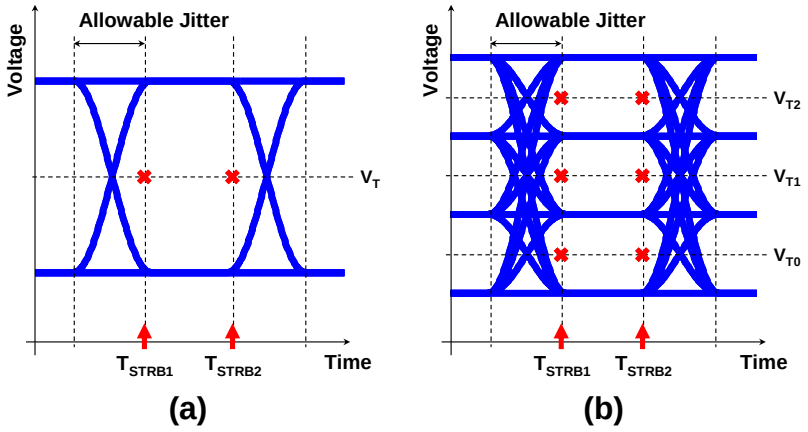

Figure 2: Jitter Generation Testing of the Tx Device. (a) Binary Signal. (b) Multi-level Signal.

2.2 Limitations of Conventional Test System

Figure 3 shows a conventional test system. The conventional system includes a pattern generator (PG), a timing generator (TG), a format controller (FC), voltage drivers (Dr), comparators (Cp), and a digital compare (DC). The PG generates test patterns input to the device under test (DUT) and expected patterns for the output signal from the DUT. The TG generates high-precision times T_{EDGE} and T_{STRB}. The voltage drivers output binary test signals with two independent voltage levels (V_{IL} and V_{IH}) according to the waveform format generated by the FC based on the test patterns and T_{EDGE}. Two independent static threshold voltages (V_{OL} and V_{OH}) are supplied to two voltage comparators, respectively. The comparators compare the signal under test with the threshold voltages and sample the comparison logic at the strobe time T_{STRB}. A pair of comparators judges the voltage level of the signal under test as to where the level lies within the three areas delimited at the two threshold voltage levels. The sampled logic is compared with their expected pattern in the DC.

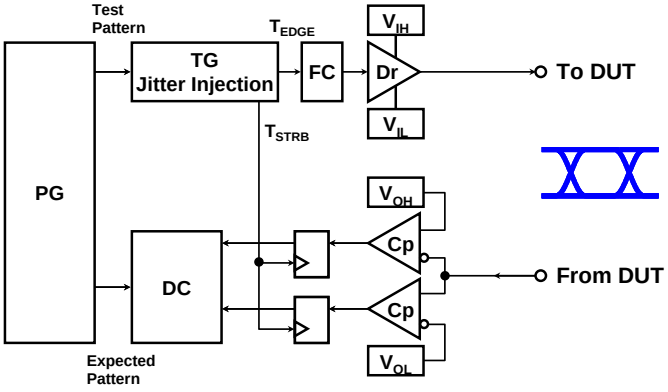

Figure 3: Conventional Test System for Binary Signals.

In order to test the functionality of the multi-level Tx device in real-time with the binary comparator, there is a method that utilizes a multiple comparator in parallel for testing the multi-level signal under test (Figure 4). However, in this parallel method, the input capacitance becomes large while increasing the number of parallel comparators. Thus, this causes the signal under test to degrade, and the accuracy of the test for the high-speed signal decreases. Furthermore, since this parallel method requires additional parts for the signal distribution such as power splitters and timing resources for compensating strobe time, skews between comparators, the testing cost increases.

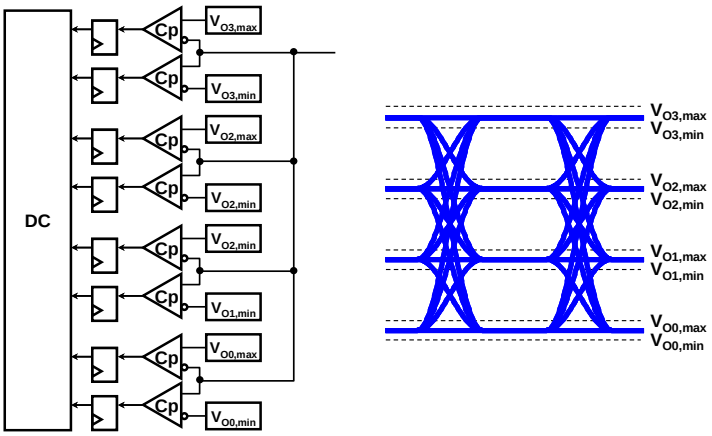

Figure 4: Comparison of Multi-level Signals with many Threshold Voltages using Binary Comparators.

3. Proposed Test System

Figure 5 shows a proposed test system for a multi-level signal [9]. This test system includes multi-level drivers and multi-level comparators based on a dynamic threshold concept. The multi-level drivers can generate the multi-level signal and control its voltage levels and signal generation times flexibly. And, the multi-level comparators can also control threshold voltage levels and strobe times flexibly. The pattern generator of the system provides a plural bit of test patterns and expected patterns that represent a multi-level logic to a multi-level driver and comparator, respectively. A timing generator of the binary test system can be reused in this system.

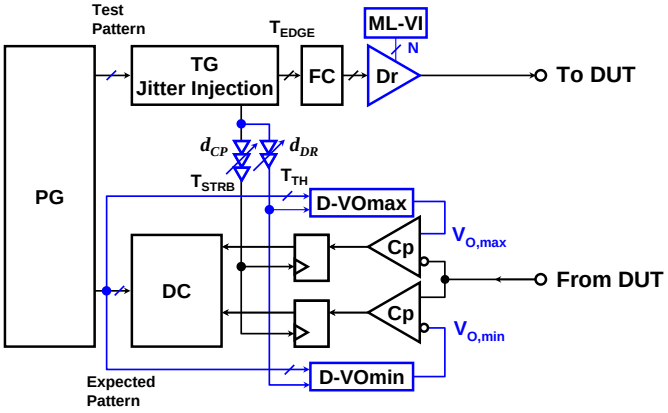

Figure 5: Proposed Test System for the Multi-level Signal.

In this section, we propose a new multi-level comparator concept. This method can perform the functional testing of the multi-level signal with the same comparator resources as a conventional binary test system by dynamically changing the threshold voltage level in response to the expected value of the signal under test. In the testing of the multi-level signal, it is confirmed that the voltage value of the signal under test is lying in the expected voltage range (Figure 6). By setting the two threshold voltages of a dual-threshold comparator to the upper limit value $V_{Ok,max}$ and lower limit value $V_{Ok,min}$ of the expected voltage value of the signal under test, the voltage margin testing of the Tx output signal can be performed at the same time as the functional testing. Compared with the static threshold comparator described in Figure 4, this method can reduce the comparator resource by 1/N times. Thus, this method reduces the input capacitance of the comparator and therefore is suitable for a test system for high-speed signals.

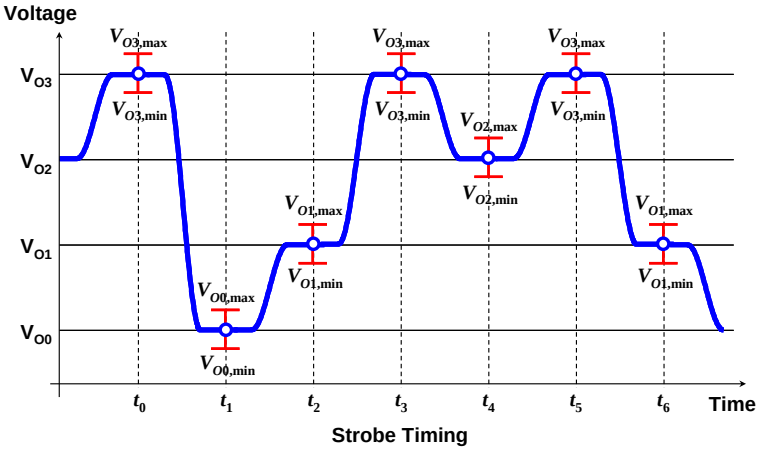

Figure 6: Concept of Proposed Dynamic Threshold Multi-level Comparator.

A multi-level signal generator (dynamic voltage output, D-VO) is utilized for generating a dynamic threshold voltage signal. Providing a dedicated threshold generator for each comparator allows for a flexible setting of the threshold voltage. By increasing the number of switchable threshold levels, this comparator scheme can be applied to testing 8-PAM (8-level), 16-PAM (16-level), and so on. Therefore, this method is scalable for the increase in the number of voltage levels within the voltage accuracy limitations of the pin-electronic design.

Furthermore, the strobe time and the threshold switching time of the proposed dynamic threshold comparator are synchronized with each other. Thus, the strobe time can always be placed after the settling of the dynamic threshold voltage. Hence, the proposed method removes the dead time in which the comparator cannot observe the correct data. For scalability and flexibility against various test rates, variable delay lines (d_{CP} and d_{DR} in Figure 5) are utilized for synchronization. And the two delay time should be controlled to minimize the impact of temperature variations.

4. Experiments

In this section, the experimental results with prototype circuit based on our proposed method are shown, and they demonstrate a concept of proposed test system for the multi-level signal.

4.1 Prototype Circuit

In order to demonstrate the proposed multi-level signal testing method, we fabricated a prototype circuit, including a 4-PAM driver and a 4-PAM comparator in 65nm standard CMOS process.

In the 4-PAM comparator, a high-speed latch comparator is used as the voltage comparator (Figure 7). In the prototype circuit, a dedicated multi-level driver is utilized for generating a dynamic threshold voltage signal for each comparator. Synchronization of the strobe time and the threshold switching time is realized by generating these times from an identical time edge with fixed delay line for simplifying the circuit design. Comparison results are de-multiplexed into low-frequency logical signal to judge pass/fail by comparing with expected patterns. Our 4-PAM comparator has a 2-way interleaved structure like the conventional system. Although it requires twice number of comparators, it can reduce the operating frequency of the comparator by half and maintain the adequate settling time of the dynamic threshold voltage.

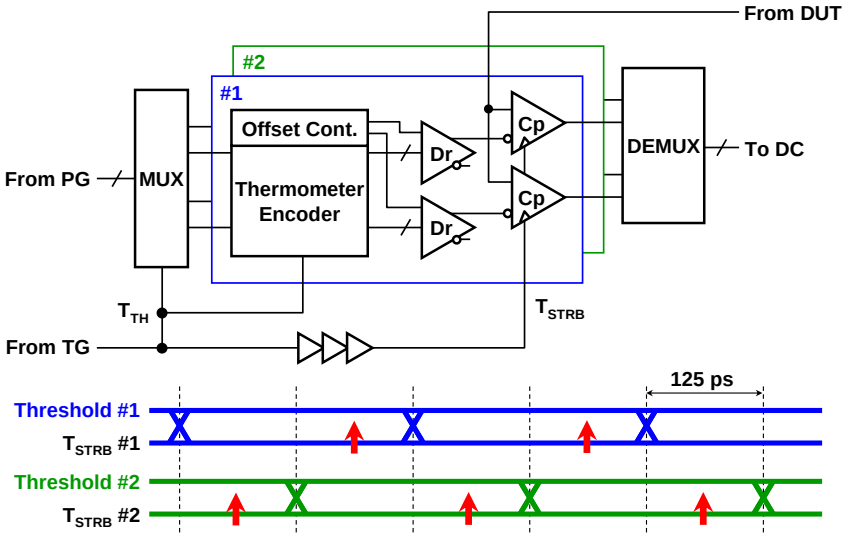

Figure 7: Prototype Multi-level Comparator Circuit.

4.2 Experimental Setup

Figure 8 shows an experimental setup. A signal generator (ROHDE&SCHWARZ SMA100A, 6 GHz) provides 1 GHz Clock to the prototype circuit as its operating reference clock. The output signal of the multi-level driver is measured by a digital real-time oscilloscope (Tektronix TDS6154C, 40 GSps). The multi-level driver output is used as a signal input to the multi-level comparator, and the threshold voltage driver built in the prototype circuit generates the threshold voltage signal of the multi-level comparator. The output signal of the multi-level comparator is provided to the BERT (Agilent N4903A, 12.5 Gbps) or the real-time oscilloscope and compared with the expected logic. The maximum operating rate of the prototype circuit is 8 giga-symbols per second (16 Gbps at 4-PAM).

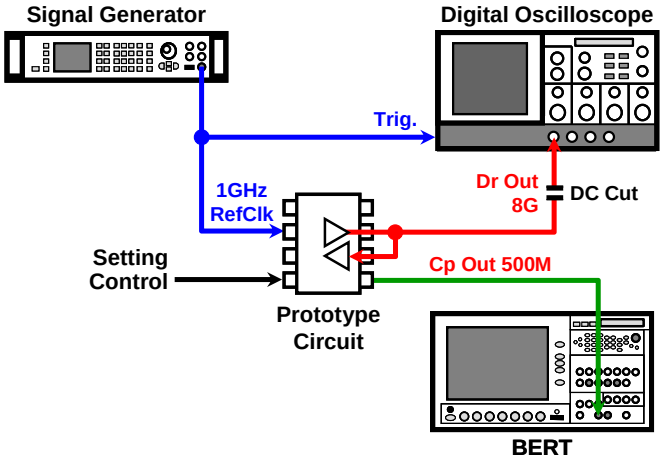

Figure 8: Experimental Setup.

4.3 Evaluation Results of 4-PAM Comparator

4.3.1 Stability of Dynamic Threshold Voltage

The stability of the threshold voltage of the dynamic threshold comparator was measured. A constant voltage signal is input to the comparator, and the cumulative distribution function (CDF) of the bit error rate in the comparison result of the comparator is measured while changing the input voltage level. The probability density function (PDF) of the comparator noise was calculated from the CDF.

In Figure 9, distributions of the comparator noise in the dynamic threshold comparator are compared between the case

when the threshold voltage is changed dynamically (dynamic mode) and the case when the threshold voltage is set to a fixed value (static mode, this corresponds to the conventional static threshold comparator). The difference between the comparator noise in the dynamic threshold mode and the static threshold mode is 1.44 mV and less than the resolution of the threshold voltage. And the standard deviation of the comparator noise in the dynamic mode is 5.35 mV_{RMS} as comparable to that in the static mode (5.09 mV_{RMS}). This result demonstrates that the threshold in the dynamic mode is as stable as that in the static mode. These comparator noises are still larger than that of conventional comparator. While the dynamic threshold is intrinsically less stable than the conventional static threshold, it is believed that the comparator noise can be decreased to half by eliminating the noise in the comparator such as the power/ground noise. This is another challenge of our next development effort.

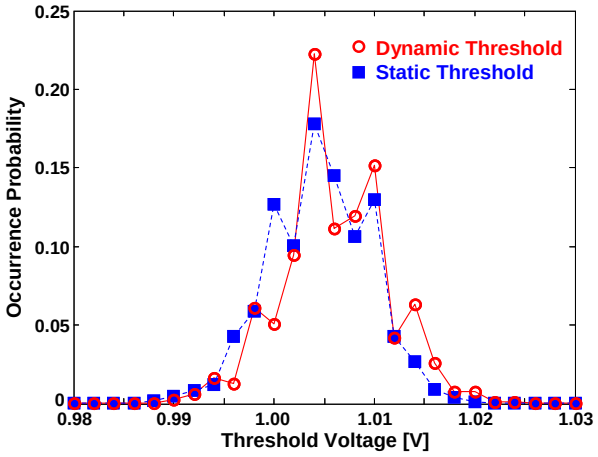

Figure 9: Comparison of Threshold Voltage Distributions in the Dynamic Mode and the Static Mode.

4.3.2 Measurement Results of Shmoo Plot

To investigate the dead time of the dynamic threshold comparator, a Shmoo plot measurement was done. The 4-PAM output signal of the multi-level driver is a looped back to the input of the multi-level comparator. While the threshold voltage level and the comparison time of the dynamic threshold comparator were swept, respectively, the Pass or Fail was measured.

Figure 10 shows a Shmoo plot measured by the dynamic threshold comparator. The dynamic threshold comparator can measure the signal under test within the comparator noise variation even at the signal transient time as well as with a conventional system. This shows that there was no comparator dead time with the proposed method.

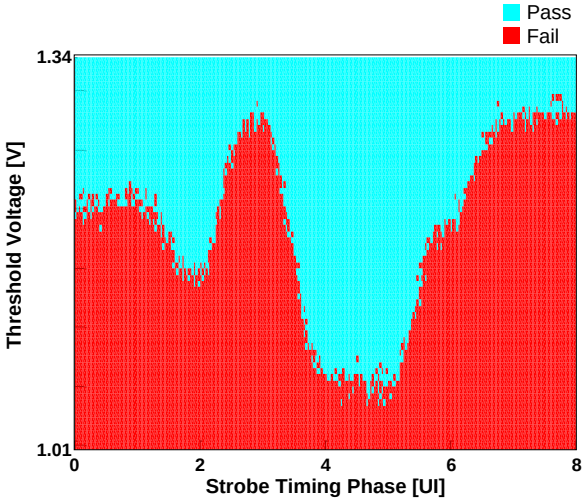

Figure 10: Shmoo plot Measured by the Dynamic Threshold Comparator.

4.3.3 Detection of Error Bit in Multi-level Signal

The experiment to confirm the circuit's ability to detect multi-level errors was done next. The 4-PAM output signal of the multi-level driver was looped back to the input of the multi-level comparator. A test pattern generator built into the prototype circuit generates a bit error (a voltage level error) repeatedly in the output signal of the multi-level driver. The error bit detection was done by comparing the erroneous signal with the expected value in real-time, by using the multi-level comparator.

Figure 11 shows the input and output signals of the comparator measured by a real-time oscilloscope in the error bit detection experiment. An error flag output signal was seen after a certain delay time (corresponding to logic processes) from the time when the error bit was injected. When no error bit was inserted, the error flag was not observed in the comparison result. Even if the error location was changed, the injected error was correctly detected by our dynamic threshold comparator. This confirms that the proposed comparator can detect an arbitrary error bit in a 4-PAM signal. The dynamic threshold comparator can compare all 4-PAM bits in real time and detect all data and voltage errors simultaneously.

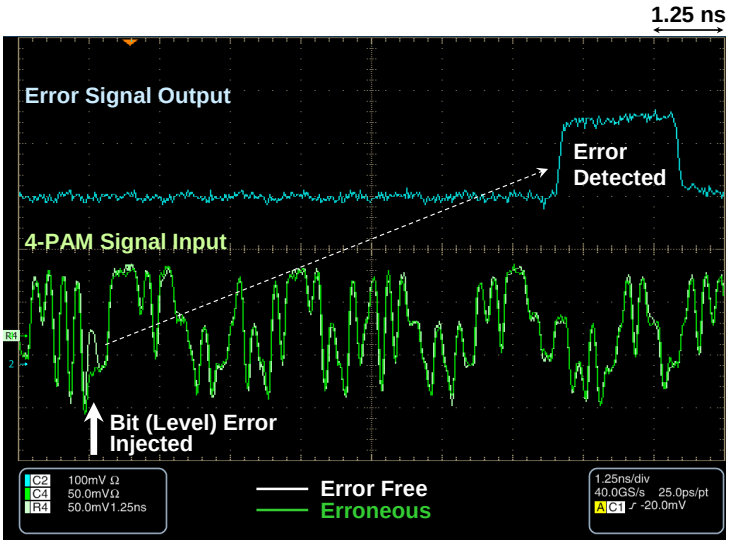

Figure 11: Results of Arbitrary Error Bit Detection.

5. Other Applications of Proposed Dynamic Threshold Comparator

5.1 Application to Binary Signal Testing

By using the proposed dynamic threshold comparator concept, functional testing of a binary signal can be carried out by only one comparator. Conventionally, as described above, in the functional testing of a binary signal, two static thresholds with different voltages ($V_{OH,min}$ and $V_{OL,max}$) comparators are used. The binary signal under test is compared with them. With a dynamic threshold comparator, a binary signal can be tested with a single comparator by setting its threshold to $V_{OH,min}$ when the expected value is High and $V_{OL,max}$ when the expected value is Low (Figure 12). This means that the number of comparator resources can be reduced by 1/2 as compared with the conventional binary test system by utilizing the dynamic threshold comparator concept. Alternatively, when the number of comparator resources is the same as the conventional system, the testing rate can be doubled by using the comparators in an interleaving manner.

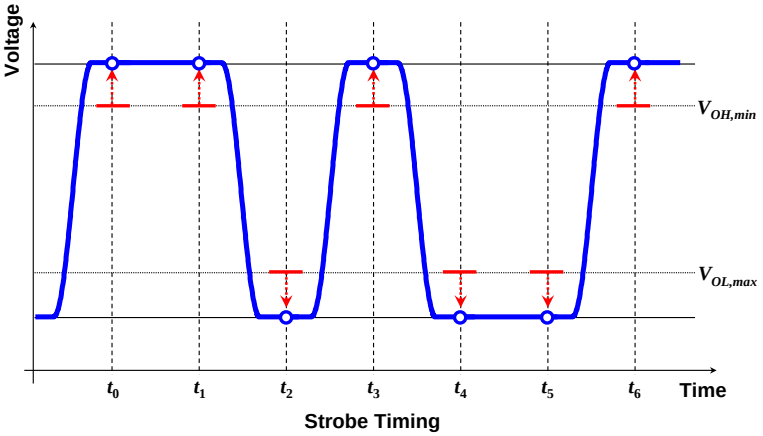

Figure 12: Binary Signal Testing with Dynamic Threshold Comparator.

5.2 Application to Analog Signal Testing

If the output voltage level of the multi-level driver and the threshold voltage level of the dynamic threshold comparator are able to be set more flexibly, the testing of an arbitrary waveform like an analog signal becomes possible. In the testing, the waveform (voltage and time) of the analog input/output signals of the SoC device are predictable. By setting the output voltage level of drivers and the threshold voltage level of the dynamic threshold comparator according to the predicted waveform, the generation of an analog test signal and the comparison between the analog output signal and the expected value become possible (Figure 13). As a result, the Go/NoGo testing of the analog signal becomes possible. We expect that the proposed method to be extended to the testing of digital modulation signals such as a quadrature amplitude modulation (QAM).

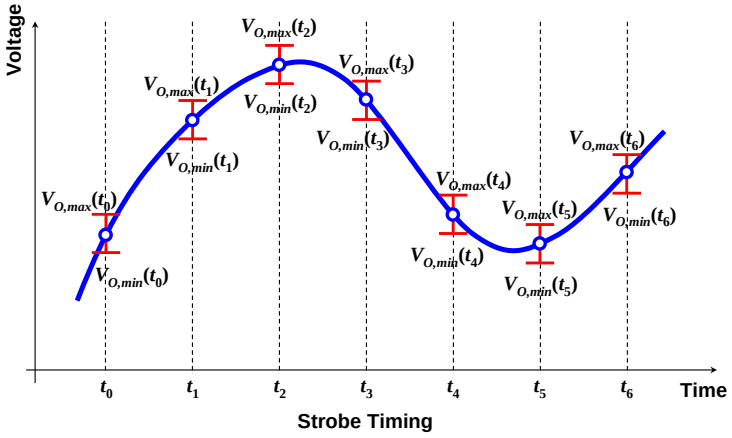

Figure 13: Real-time Testing of Analog Signal with Dynamic Threshold Comparator.

6. Conclusion

In this article, a method for testing devices with multi-level signal interfaces was proposed. The proposed system has multi-level comparators based on a new concept. The multi-level comparator can realize the real-time functional testing of a multi-level signal by switching its threshold voltage levels dynamically in response to the expected value of the signal under test. As compared with a conventional static threshold comparator, this dynamic threshold comparator method reduces the number of comparator resources and is suitable for a system testing a high-speed signal. Experimental results with the prototype circuits show that the proposed system can achieve a real-time functional testing for the 16 Gbps 4-PAM signal and therefore shows the feasibility of the approach. This system is applicable to real-time testing of both binary signals and multi-level signals and is scalable to increase the number of voltage levels. Reducing noise and jitter of the multi-level comparator is a future challenge for this development.

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