Hideo Okawara's
Mixed Signal Lecture Series

DSP-Based Testing – Fundamentals 23
Centering

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Preface to the Series

ADC and DAC are the most typical mixed signal devices. In mixed signal testing, analog stimulus signal is generated by an arbitrary waveform generator (AWG) which employs a D/A converter inside, and analog signal is measured by a digitizer or a sampler which employs an A/D converter inside. The stimulus signal is created with mathematical method, and the measured signal is processed with mathematical method, extracting various parameters. It is based on digital signal processing (DSP) so that our test methodologies are often called DSP-based testing.

Test/application engineers in the mixed signal field should have thorough knowledge about DSP-based testing. FFT (Fast Fourier Transform) is the most powerful tool here. This corner will deliver a series of fundamental knowledge of DSP-based testing, especially FFT and its related topics. It will help test/application engineers comprehend what the DSP-based testing is and assorted techniques.

Editor's Note

For other articles in this series, please visit the Verigy web site at www.verigy.com/go/gosemi.

Positioning of Waveform

In mixed signal tests assorted waveforms, such as sinusoidal, triangle, trapezoidal, square waveforms, a single cycle, multiple cycles of such waveforms, are captured by a digitizer/sampler and a DUT ADC. Captured waveform would be graphically displayed on an appropriate display tool, and test engineers would make up a strategy how to analyze the waveform and extract necessary parameters. The location of captured waveform is not always fixed in the unit test period (UTP) window. If you need to evaluate the shape of the waveform, you may need to adjust the location of the waveform appropriately. For example, a template test must check the captured waveform to exactly fit inside the given limit template. Since the pass/fail judging task is processed by a computer eventually, not by your eyes, it is important to make your target signal in the suitable position. Shifting the waveform data left and right in the UTP window is the theme of this article. This is applications of FFT and IFFT.

Square Wave and Its Bin#1 Sinusoid

Let's examine the fundamental sinusoid's phase of a square clock waveform sitting in a 4 different locations in the UTP window. Figure 1 illustrates the 4 cases of a clock pulse (yellow) sitting in different locations. The blue lines show their bin#1 sinusoid of FFT results. "Phase" in each case shows the phase value of the sinusoid. Probably the most possible location for easy data processing is the case of "Phase=$-\pi$". The logic high pulse is centered so that the rising/falling edges of the waveform would be located at approximately the 1/4 and 3/4 of UTP.

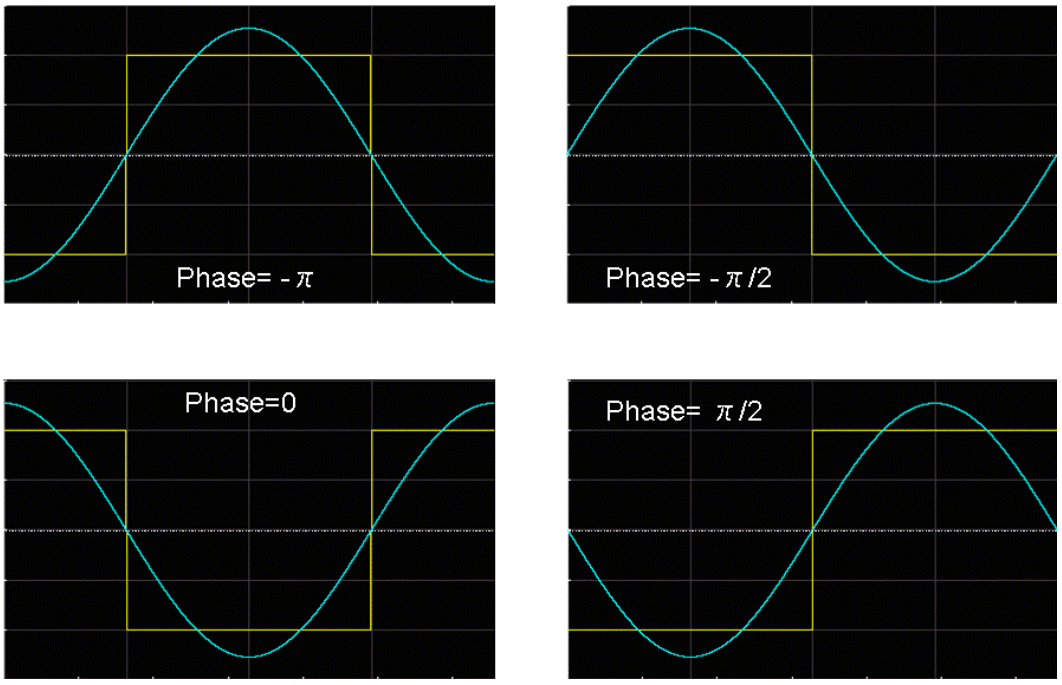

Figure 1: Clock Pulse Locations and Their FFT Bin#1 Sinusoid's Phases

Case 1: Rise/Fall Time

The Yellow line in Figure 2 illustrates a measured clock waveform. Your eyes can easily recognize where the rising and falling edges are located.

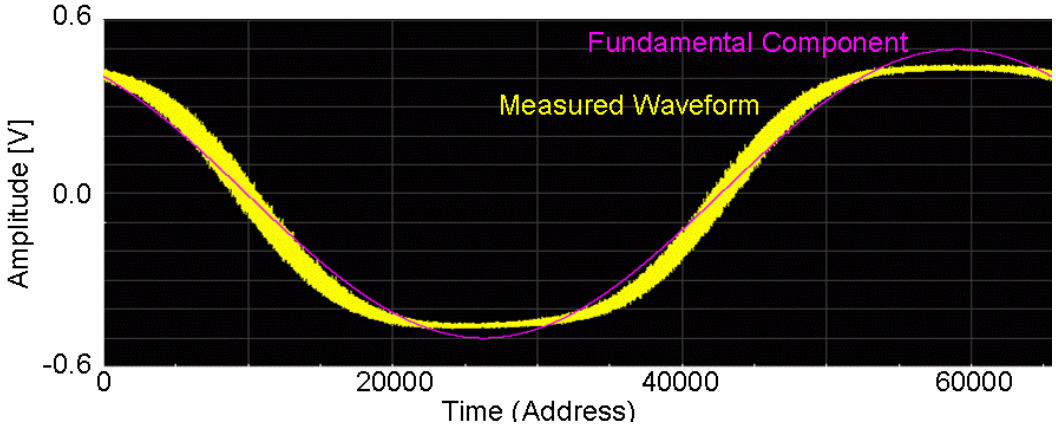

Figure 2: Measured Clock Waveform

So you can point out the correct slopes and calculate the rise/fall times. Location of waveform is not always captured at the fixed position every time. A computer in ATE must process the waveform appropriately without your interactive advice. Therefore the clock waveform should be moved left or right to sit in an appropriate location as Figure 3. If the waveform is located in the expected position every time, the data processing could be simple and robust.

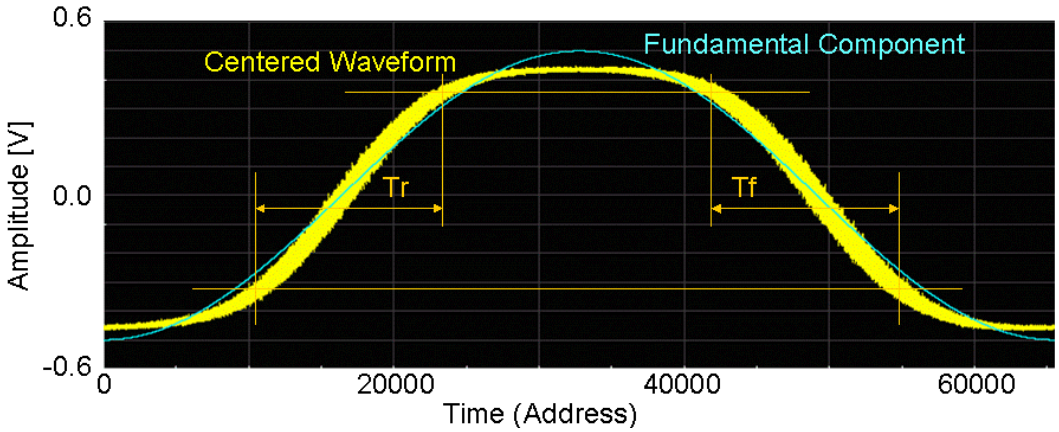

Figure 3: Centered Waveform

By applying FFT to the clock signal, the fundamental tone of the waveform is shown in the red line in Figure 2. As discussed in the previous section, the target phase is $-\pi$ [rad] which is shown as blue line in Figure 3. By comparing the phase difference between the fundamental components in Figures 2 and 3, you can find out how many addresses the clock waveform should be moved left or right. The data size of UTP corresponds to 2π [rad] so that the phase difference is normalized by 2π and it is substituted address difference. Then you can shift and rotate the waveform.

Case 2: Pulse Template

Figure 4 illustrates a pulse mask or template for an AMI[1] signal for a data communication system. The two lines show the upper and lower limit of the signal waveform. A measured signal waveform is tested to fit in the given limit lines.

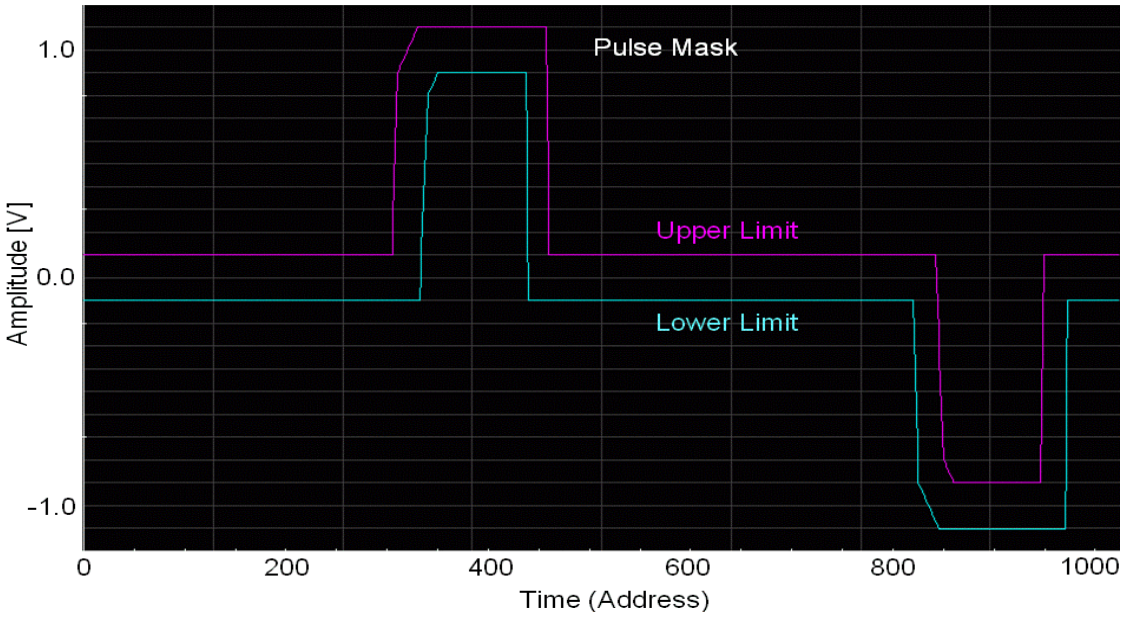

Figure 4: AMI Pulse Template

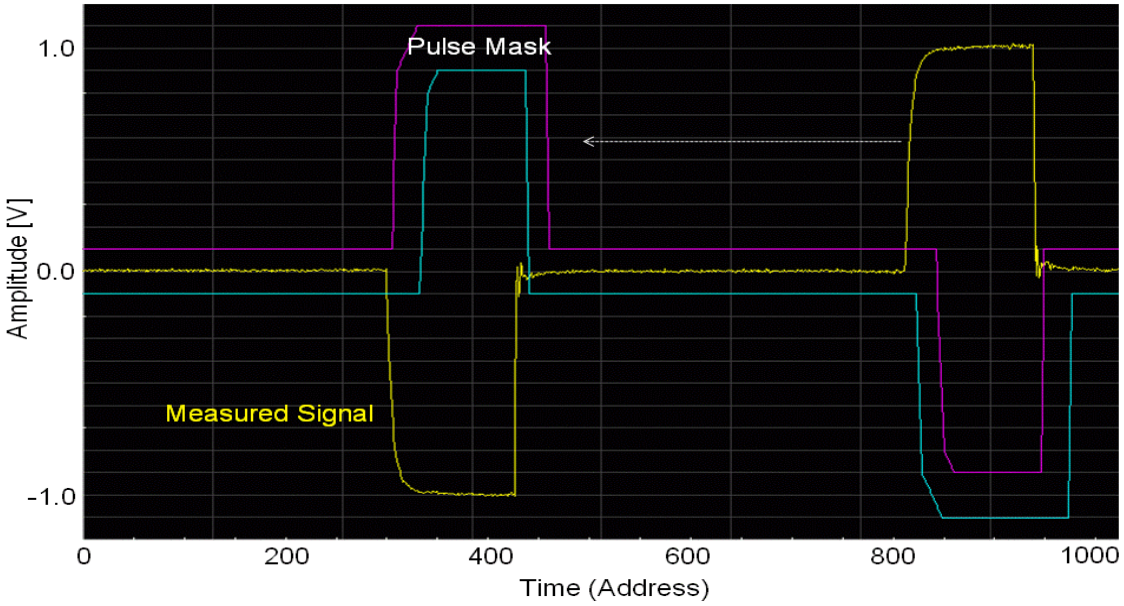

Figure 5: AMI Pulse Captured

[1] Alternate Mark Inversion: A type of digital signal used in legacy wired communication. Logic 0 is fixed 0V but logic 1 changes its physical polarity such as +1V and -1V alternately in order to make DC level balanced. This operation enables the signal to go through transformers in the path.

The yellow line in Figure 5 is an actually captured AMI test signal waveform, which looks good but is far off the template location. So firstly you should move the signal trace left appropriately to the mask location. The simplest method to do that is to search the rising edge of the positive pulse, measure the distance to the target location and shift the waveform data by estimated steps of address. However, automatic edge search may not work correctly when the signal is noisy.
Let's think of an elegant method to address this task. Performing FFT/IFFT to the upper/lower templates and the measured waveform reconstructs the fundamental components of them illustrated in Figure 6 as one-cycle (bin#1) sinusoidal waveforms.

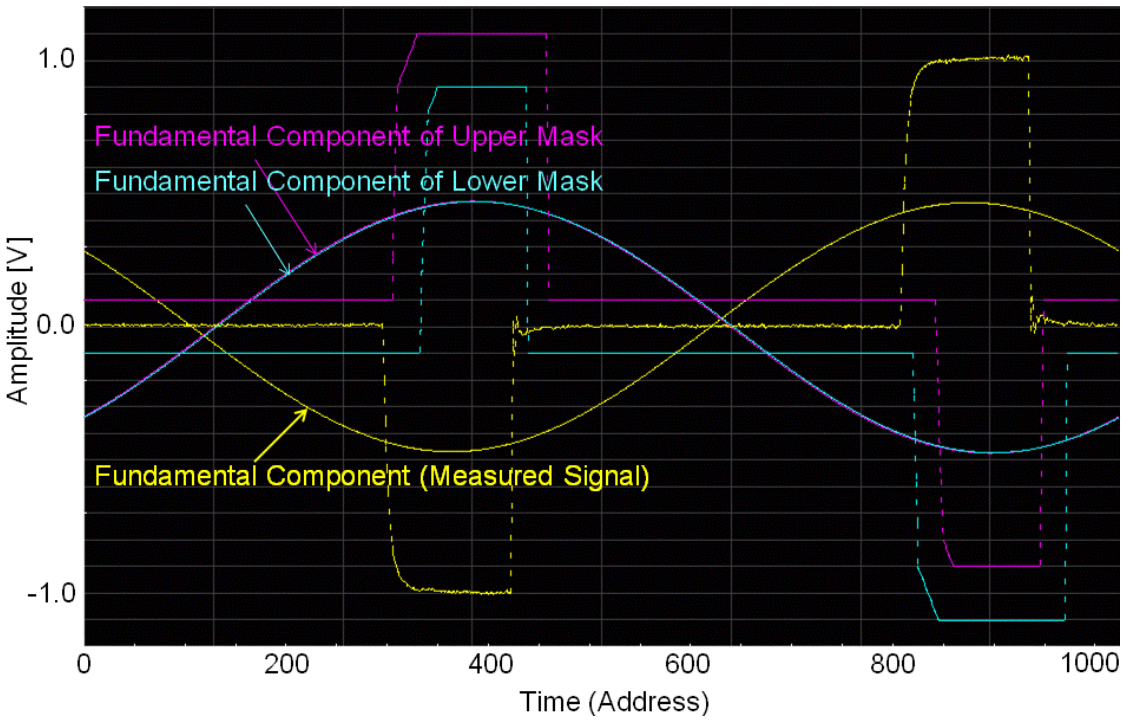

Figure 6: Fundamental Components of Masks and Signal

The fundamental components of the masks have almost the same phase. So the average phase of the mask lines and the phase of measured pulse are compared with each other. By calculating the phase difference of the fundamental sinusoids, and estimating how much steps the measured waveform should be moved, the measured signal can be settled inside the templates as Figure 7 illustrates (green line).

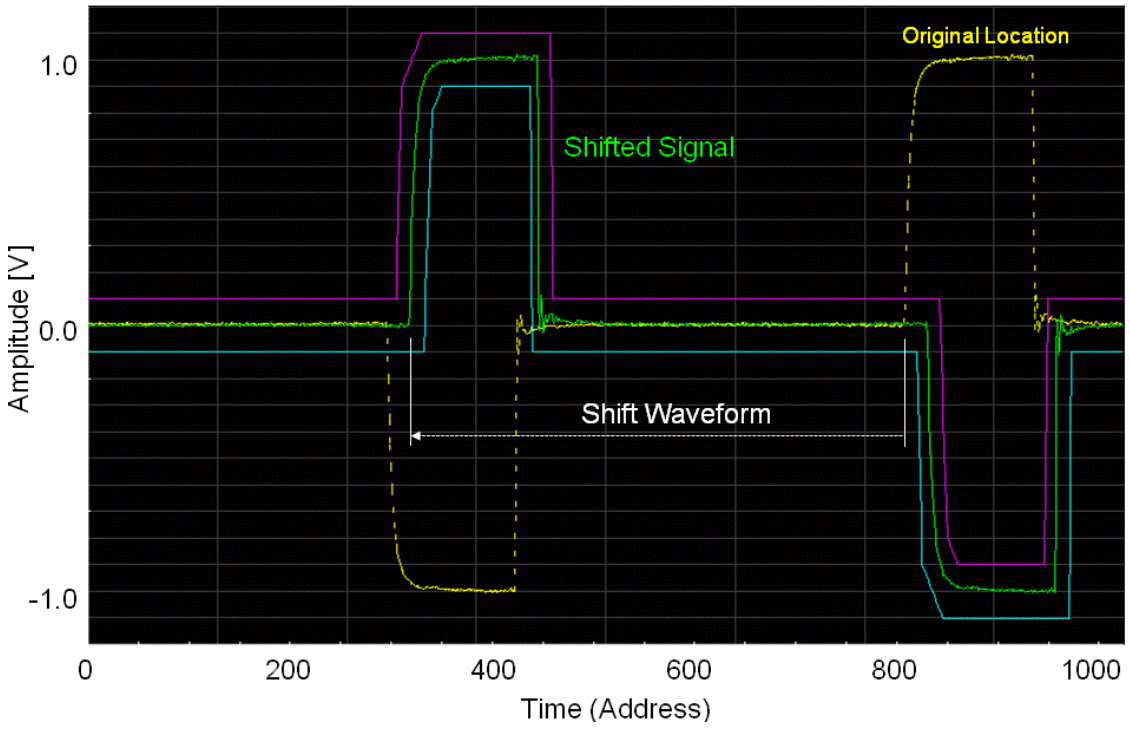

Figure 7: Signal Shifted in the Template

Case 3: Eye Pattern

Figure 8 illustrates an image of an eye mask test in high-speed digital signals. Firstly an eye pattern (or diagram) is constructed, and then the eye opening is tested not to violate the given eye mask.

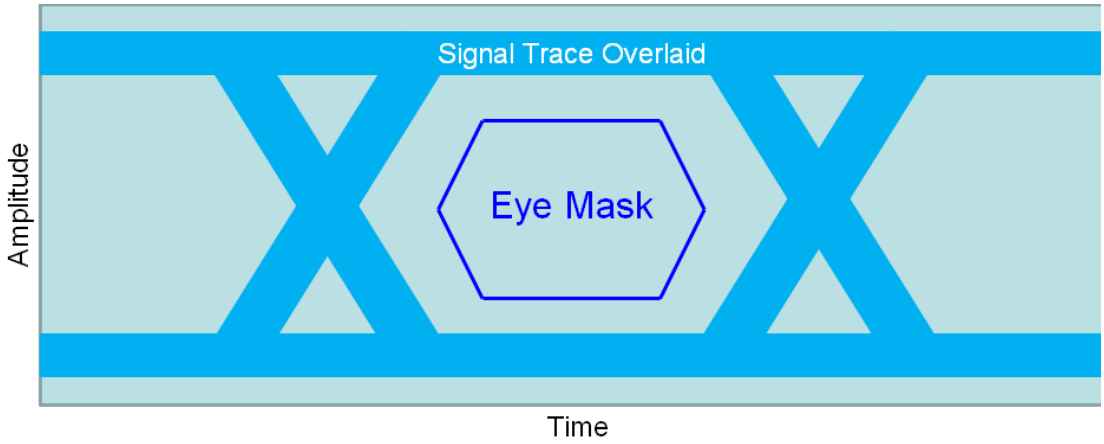

Figure 8: Eye Pattern and Mask Specification

Figure 9 shows a primitive eye pattern captured and it cannot be tested with the eye mask automatically without location manipulation.

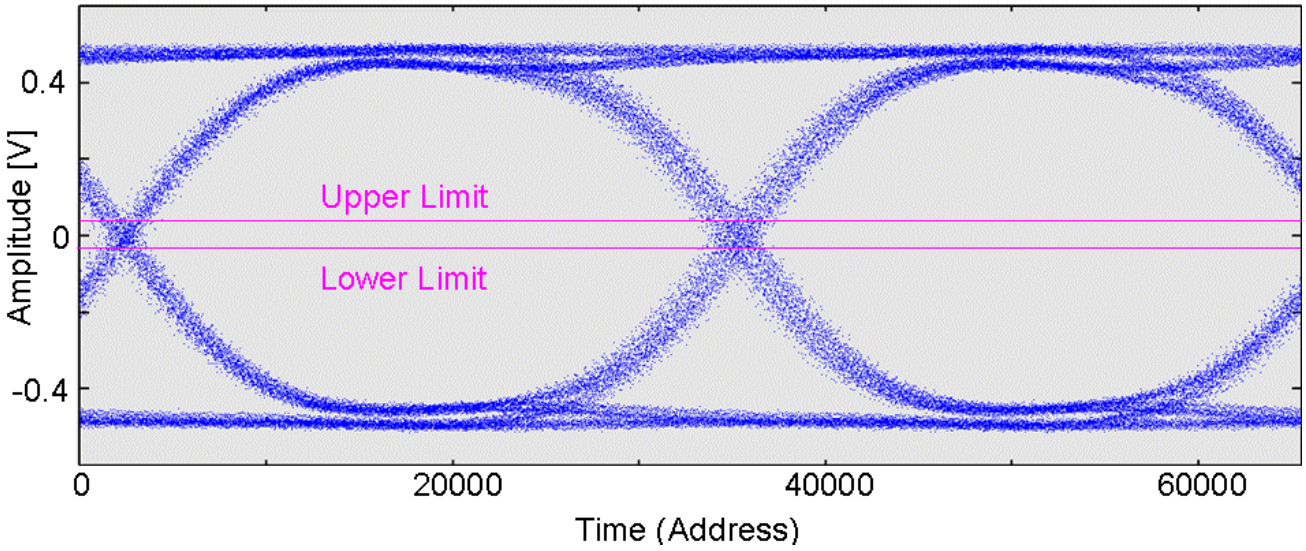

Figure 9: Primitive Eye Pattern

At first, the eye should be moved forward or backward appropriately to be located at the center of the UTP. In order to get the clue of the eye location, data points distributing in the vicinity of the crossing-edges are collected by employing temporary upper and lower limits drawn in Figure 9. As Figure 10 illustrates, when a data point falls between the slit in (a), the newly introduced array is marked one as (b).

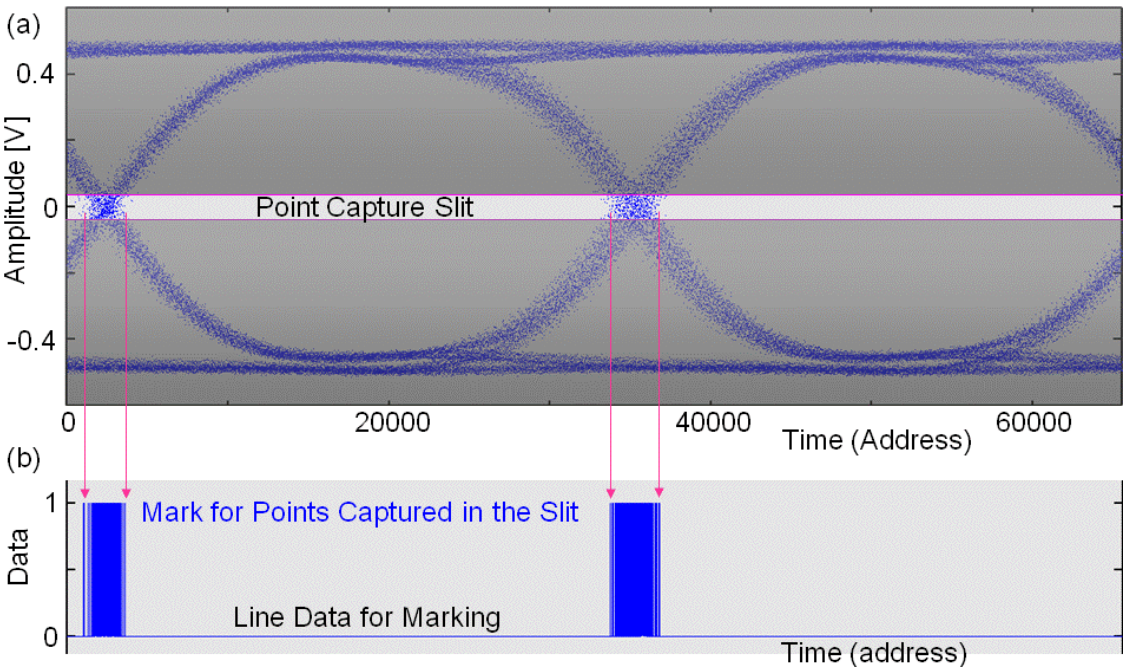

Figure 10: Edge Detection Slit and Generated Mark Signal

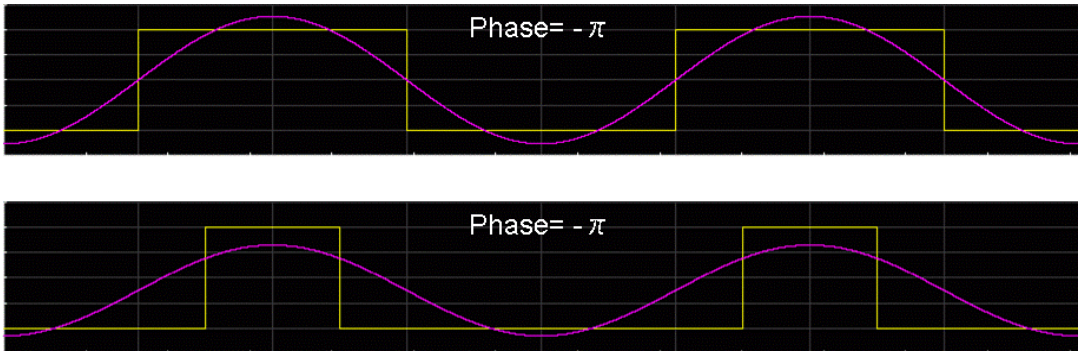

Figure 11: 2-cycle Clock Pulse and the fundamental Sinusoid (Bin#2)

Figure 11 illustrates 2-cycle clock waveform and its primary component as FFT bin#2. The phase of the sinusoid is $-\pi$. By applying FFT to the mark signal in Figure 10(b), the bin#2 sinusoid is shown as the red line in Figure 12(a). The expected location of the mark signal is shown as the yellow line in (b). The phase difference between the red lines in (a) and (b) can be interpreted into the time axis address difference. Then the primitive eye pattern in Figure 9 can be shifted forward or backward to be settled in the center of the UTP as Figure 13. Then it can be tested with an eye mask data.

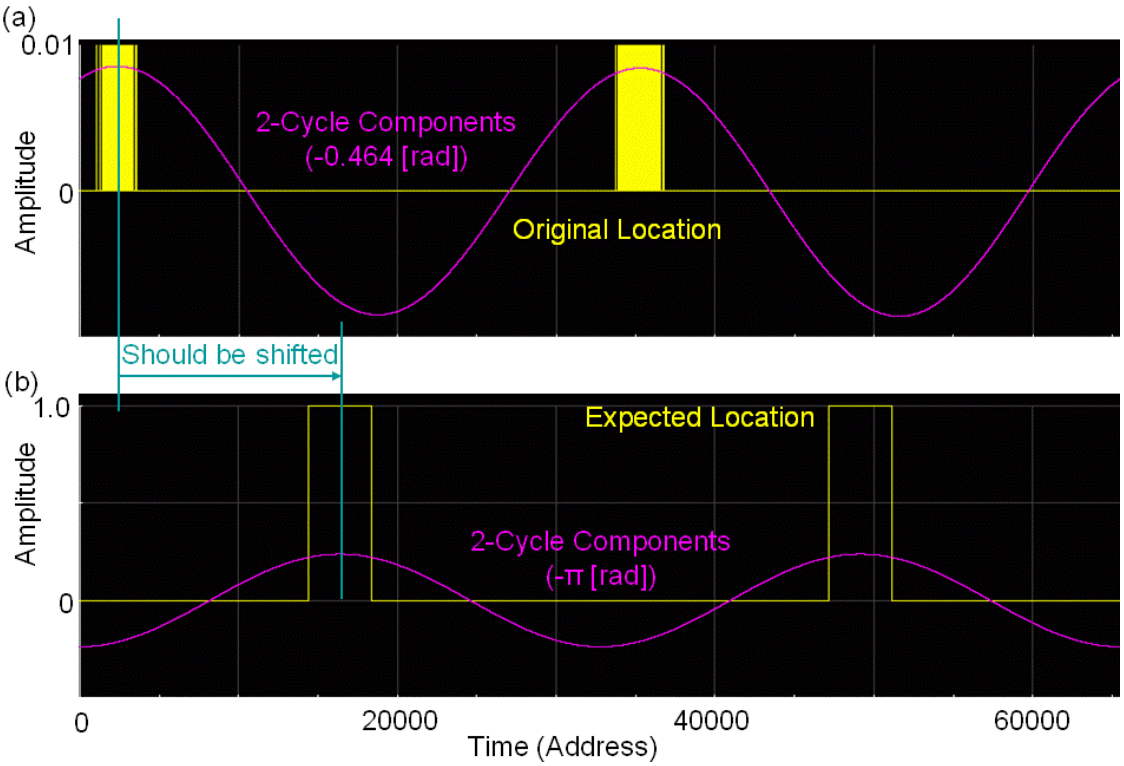

Figure 12: 2-cycle Component of Mark Signal

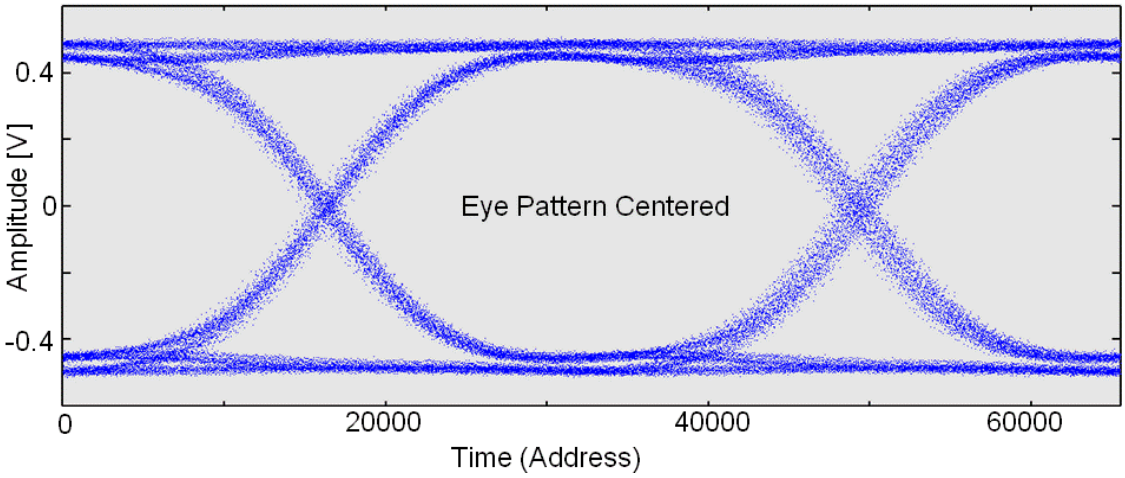

Figure 13: Eye Pattern Centered