

Question: “What is the difference between 'Boundary Scan Test' and 'Scan Test'?”

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Often devices support both scan test and boundary scan test. What is the difference between 'Boundary Scan Test' and 'Scan Test'?

Answer:

Scan test is used to test the internal logic of the DUT while boundary scan test originally was focused on controlling the IO pins in order to allow testing interconnects between chips on a board.

As for scan test, the boundary scan architecture is also based on a chain of special cells. Such a cell provides a shift mode and is called “boundary scan cell” (BSC). Usually, boundary scan is implemented as follows: To each primary input, primary output and bidirectional primary IO a BSC is assigned. For each output and bidirectional IO one more BSC is added that allows enabling and disabling the corresponding output driver during boundary scan test. All these BSCs are concatenated forming a single boundary scan chain.

A boundary scan chain can support the following features, depending on the type of the primary IO and the type of the BS:

- The BSCs capture the value applied to the primary input/IO.
- The BSCs provide to the internal logic of the device the value stored in the cell instead of the value applied to the primary input/IO.
- The BSCs capture an output value forced by the internal logic.
- The BSCs provide to the primary output/IO a value that has been stored in the cell instead of the value forced by the internal logic.

Beside board tests like interconnect checking, classical test scenarios for boundary scan are:

- Capture values applied to the inputs (for example, to check the signal path from the pins to the internal logic.)
- Force values at the outputs (for example, to characterize output drivers of a device).
- Switch off all output drivers of the device (for example, to perform latch-up tests).

The IEEE 1149.1 standard describes the boundary scan architecture including a test interface of 4 or 5 pins, that is called “Test Access Port” (TAP), a test controller and certain boundary scan features. In particular, IEEE 1149.1 specifies how to control the settings of the BSCs and how to serially load and unload the values stored in the BSCs, i.e. in the boundary scan chain. On a board with several chips implementing TAPs and boundary scan according to the standard, this architecture allows a simple, serial access to all boundary scan chains via a single interface.

In recent years the IEEE 1149.1 standard has been enhanced by new standards, for example specifying boundary scan solutions for analog pins, for high speed differential pins, or for reduced pin count test.

For scan tests such a standard does not exist. So very often a boundary scan test controller according to standard IEEE 1149.1 is also used to enable and configure scan test modes. In order to achieve this, the boundary scan test controller is enhanced to support non-standard instructions, while no changes to the TAP are required.