Solving MIPI D-PHY Transmitter Test Challenges

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Abstract

MIPI stands for "Mobile Industry Processor Interface", which provides a flexible, low-cost, high-speed interface solution for communication links between components inside a mobile device. With more than 100 companies backing this emerging standard, MIPI is expected to be widely adopted for smart phones and similar application-rich networked devices, as well as in personal digital assistants (PDAs), and other consumer electronics. [1]

This paper, which complements another one published in the December 2008 issue of go/semi newsletter, elaborates the transmitter test solution for the MIPI D-PHY standard. On top of the source-synchronous nature of data transmission, it's the need to provide flexible tester receiver modes that makes the MIPI transmitter testing a non-trivial task, as it requires:
1. True differential and independent single-ended comparators per differential pin pair
2. Multi-level comparator thresholds
3. Correct signal termination (both terminated and unterminated receive modes)

In particular, the correct signal termination requires special attention, since the termination must be even changed on the fly within a pattern, which requires not only flexibility on the tester pins, but also some advanced techniques when programming the V93000. In fact, this can be achieved by combining tester receive edges with the driver's data drive actions and High-Z switch actions while carefully compensating the intrinsic delay, round trip delay, and fixture delay. To this end, test engineers will learn all the subtleties to properly terminate MIPI signals for multi-level waveform detection.

Key Words – MIPI, D-PHY, transmitter test, multi-level detect, change termination mode

1. Introduction

The Mobile Industry Processor Interface (MIPI) is an increasingly adopted high-speed source-synchronous interface for communication links between components inside a mobile device. Due to its flexible, low-cost and high performance nature, it is widely applied for smart phones, rich networked devices, PDAs and other consumer electronics.

The MIPI D-PHY standard comprises two data transmission modes: a low-swing high-speed differential mode for data transmission, and a large-swing low-power single-ended mode for control purposes [2]. Since those two modes differ significantly in their characteristics, MIPI requires a very flexible test solution to ensure comprehensive test coverage.

MIPI receiver test, for example, require equipment being able to generate multi-level signals. The challenges associated with that and how they can be addressed by the V93000 digital cards are the primary focus of a paper published in the December 2008 issue of go/semi newsletter [3]. To further explore the topic on MIPI test, this paper is focusing on the MIPI transmitter test.

2. ATE receiver requirement for DUT transmitter test

Besides addressing the source-synchronous nature [4] of the MIPI interface, the requirement to provide flexible tester receiver modes makes the MIPI transmitter test a non-trivial task.

2.1. Differential and independent single-ended comparators per differential pin pair

Being an ideal solution for MIPI test, the V93000 Pin Scale 800 and Pin Scale 3600 digital cards are capable of providing both true differential and single-ended comparators. When coming to practice, for each differential lane pin pairs following the rule of channel numbers 10101/10103, 10102/10104 etc. should be utilized to provide two individual single-ended receiver inputs for taking in Low-Power signals as well as to form true differential receiver inputs for taking in High-Speed signals. In addition, each individual receiver pin should be specified as an IO pin. Hence, native (close to real application) testing can be achieved if different data transmission modes are tested separately in individual test suites, i.e. switching between differential and single-ended receivers.

2.2. Multi-level waveform detection with different receiver termination modes

For testing different MIPI signal modes as depicted in Figure 1, two different ways of implementation based on different testing requirements can be brought up. The first choice, which is more straight-forward, is to separate the test items for High-Speed and Low-Power signals into individual test suites as discussed in paragraph 2.1.

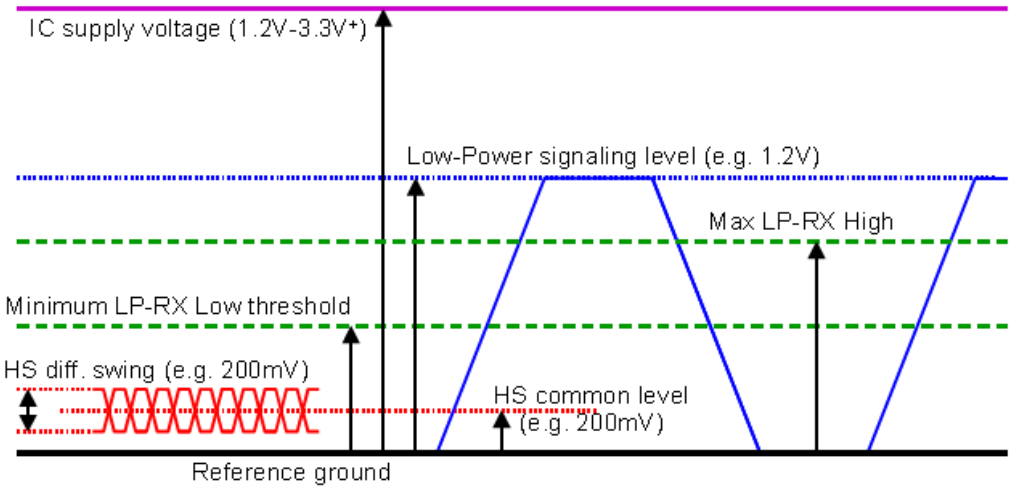


Figure 1: MIPI D-PHY line levels [2] (single-ended view)

However, if it is required to test both signaling modes within one test suite (i.e. within the same pattern execution), then there are two possibilities.

As the first choice, the user can define different level sets for the two different types of signals and use the firmware command CLEV to change between different level sets.

By means of this approach, it is possible to change between differential receiver mode and single-ended receiver mode. Also the compare thresholds of both High-Speed and Low-Power signals, which are defined in separate level sets, can be precisely programmed. Nevertheless, since the CLEV command inserts a number of break and hold vectors, there will be a certain period where the tester receiver is “blind” and unable to see actual signal transitions from High-Speed to Low-Power mode and vice versa when the data transmission mode change occurs within the same pattern; this sets the limitation of changing tester receiver mode on the fly.

The second method of implementation is comparably a little more complex. Unlike the previous one, the second approach employs a single level set for both High-Speed low-swing differential signals and Low-Power large-swing single-ended signals. Consequently, no break and hold cycles will occur, i.e. the tester receiver keeps track of every DUT cycle and is able to compare these two complete different High-Speed and Low-Power signals as well as transitions between them truly on the fly.

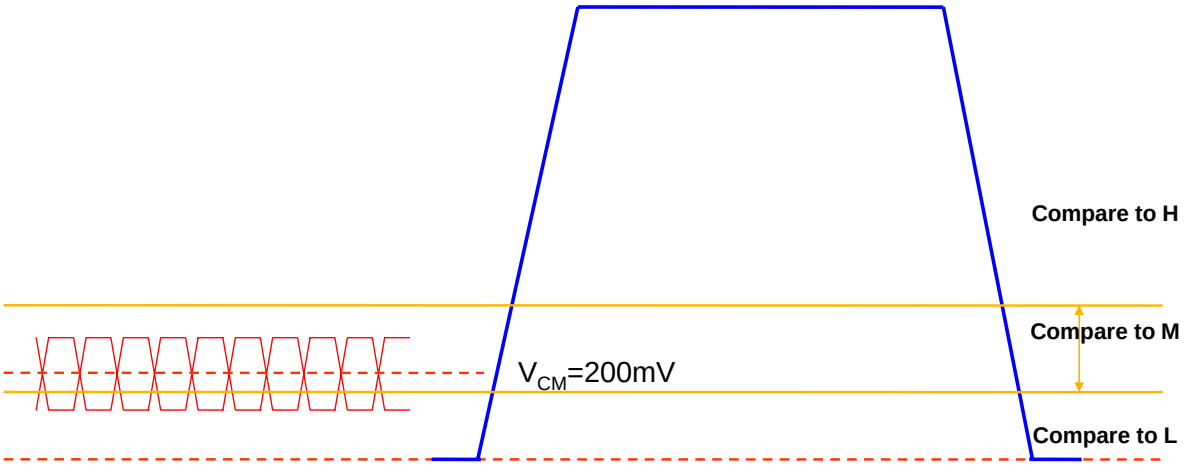


Figure 2: Multi-level signal comparison

While the two types of signal swings differ significantly from each other, multi-level signal comparison can be accomplished by introducing a “Compare to M” (Compare to Intermediate) action as shown in Figure 2. The threshold “M” stands for the intermediate range between compare thresholds “H” and “L”; here it is utilized to compare the High-Speed logical 1. The compare threshold “L” is used to judge both the levels of High-Speed logical 0 and Low-Power logical 0. Compare threshold “H” is used to distinguish the Low-Power logical 1 from the High-Speed logical 1. The actual value of compare threshold “H” is typically between 300mV and 1V and is easily adjustable according to the test case of a real device.

In addition, in order to cope with the multi-level signal comparison requirement, the tester receiver also needs to be able to switch between different termination modes on the fly. This demands not only flexibility in the tester pin electronics, but also some advanced techniques when programming the tester.

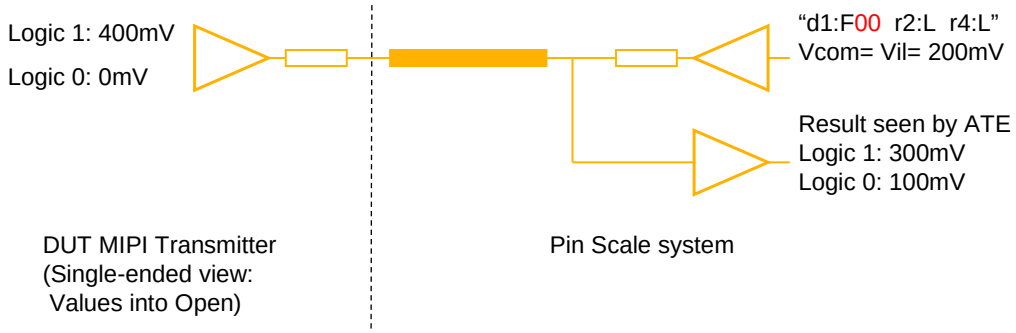


Figure 3: Terminated ATE receiver for High-Speed signal

Figure 3 illustrates the situation when the MIPI transmitter generates a High-Speed signal with a peak-to-peak voltage swing of 400mV into open, which is equivalent to a 200mV swing into 50Ohm termination according to the specification (single-ended view). The signal propagates through the transmission line and is further terminated to the common mode voltage of 200mV.

This is achieved by a properly determined drive edge action which sources the common mode voltage for the tester receiver pins. As a result, the 100mV to 300mV swing (single-ended view) is observed at the tester receiver side.

Once the drive action of edge d1:F00 is defined in the wavetable to activate the termination on the receiver pin, as shown in Figure 3, it will switch off the High-Z state on the internal driver side and set the driver to source a voltage that represents a logical 0 to the internal receiver side. Therefore an appropriate voltage value of "Vil" that equals to the common mode voltage on the receiver side must be specified in the level spec.

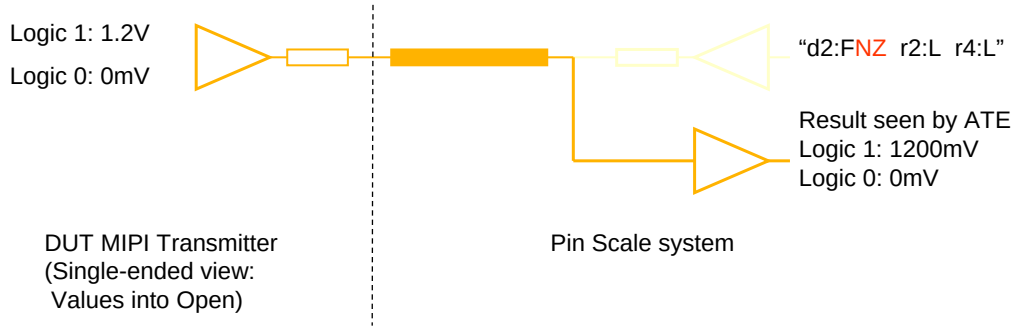


Figure 4: Unterminated ATE receiver for Low-Power signal

Consequently, when the Low-Power signal is fed into the pin electronics, the termination of the receive pin must be switched off by means of turning the internal driver into High-Z state. In this state the internal driver can be omitted (apart from some leakage current which is still flowing but not affecting the principle explained herein) from the pin electronics as shown in Figure 4.

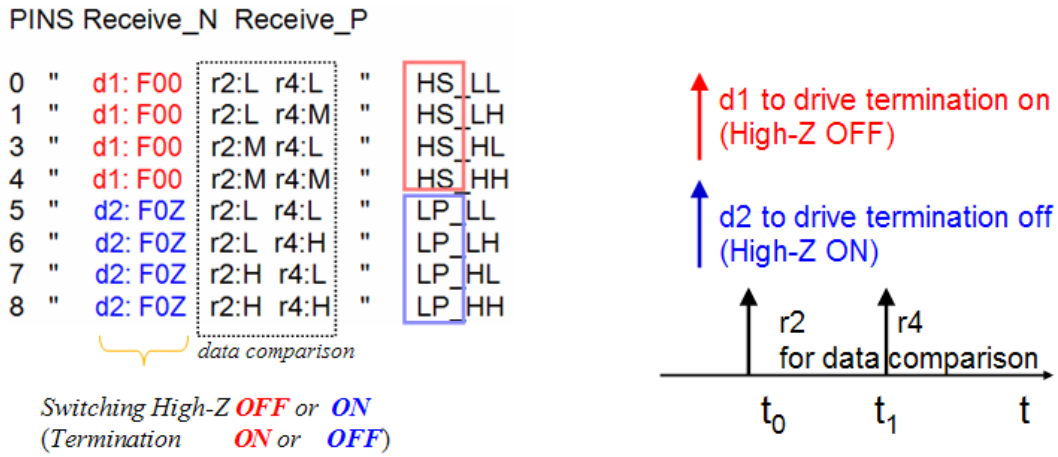


Figure 5: Suggested waveforms for tester receiver pins

As an example, Figure 5 depicts how the wavetable may look like for the receiver pin pairs, here the "r2" and "r4" receive edges are adopted for normal compare action, while "d1" and "d2" drive edges are explicitly defined and carefully compensated to precede "r2" to switch the termination mode on the internal driver side. Attention must be paid to select different drive edges (e.g. d1:F00, d2: FNZ) to switch the termination mode to either on or off, because both termination switching actions exhibit different intrinsic delays which need to be considered. The termination mode of the receive pin corresponds inversely to the High-Z state on its internal driver side.

3. Timing compensation for ATE receiver mode switch

It is known that High-Z on/off state changes on the driver side [3] lead to certain intrinsic delays which must be compensated. Moreover, there are additional factors which need to be considered for such termination drive actions of a receiver pin.

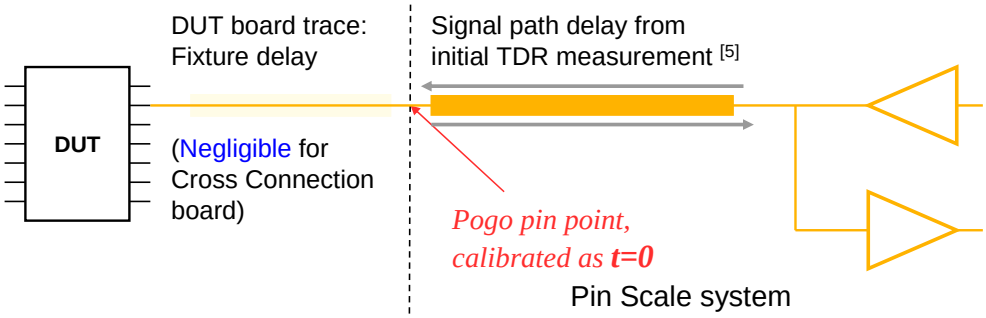


Figure 6: Signal propagation path with the cross connection setup

For an ATE system, its timing is either referred to the DUT socket (including fixture delay compensation) or to the pogo pins (without fixture delay compensation). In other words, the exact moment when a signal (transition) comes out of the pogo pin is defined to be the reference point as "*t=0ns*". Therefore, the ATE system needs to generate the signal in advance of the nominal transition point the user has programmed in order to compensate the signal path delay as depicted in Figure 6. Since switching of the termination mode occurs inside the receive pin, the signal is transmitted internally on a very short signal path compared to the length of the normal signal path through the pogo pin, which results in a very small round trip delay for the signal to propagate.

3.1. Receiver channel compensation with cross connection setup

The V93000 system calibration takes care of the signal path delay from the channel driver/ receiver to the pogo pin, and ensures that the point in time the signal appears at the pogo pin is correctly referred to t=0.

Therefore the overall amount of time which needs to be compensated, based on the setup, for either "d1" or "d2" covers the effects of:
- Intrinsic delay of switching on/off termination for the receiver pin
- Timing advance due to different round trip delay for signal change inside receiver pin.

As a rule of thumb, the round trip delay for PS800 is about 5-6ns, which means the internal driver is programmed approximately 6ns in advance than expected for the signal to appear at the internal receiver in time. As a comparison, the intrinsic delay raised by changing the termination of an internal driver takes roughly 2ns lag. Since the intrinsic delay of switching into or out of the High-Z state is different, the user needs to perform the compensation on a per-pin and per-edge (High-Z on/off) basis. The sum of signal path delay (per-pin) and intrinsic switching delay (per-pin, per-edge) constitutes the overall compensation value to be entered in the pin attributes file.

As a quick way to measure the overall compensation value, the user can program a constant voltage output at a driver channel, which is by means of the cross connection board looped back to a receiver channel, and on the other side simply switch the termination modes of that receiver channel to observe the difference compared to the expected timing.

Figure 7: Switch into unterminated ATE Rx mode (uncompensated)

Figure 7 illustrates the waveform seen by the receiver when the receiver is switched from terminated to unterminated mode. In this example, the driver is programmed to source a static signal at a voltage level of 400mV to the receiver, which signal path is as depicted in Figure 3, and the receiver detects a terminated signal voltage level of 300mV. When the receiver mode is switched to unterminated, the electrical characteristic of the receiver changes to the one shown in Figure 4, and as a result, a 400mV unterminated static signal is detected. With reference to the 50% transition point, a time delay of 3.36ns can be observed.

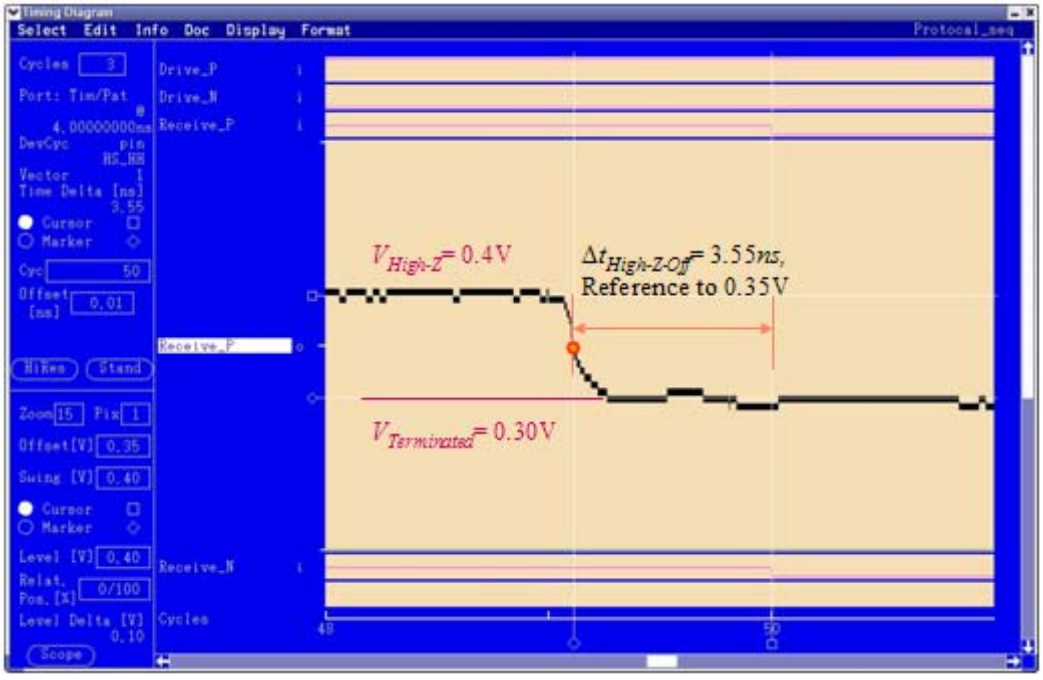
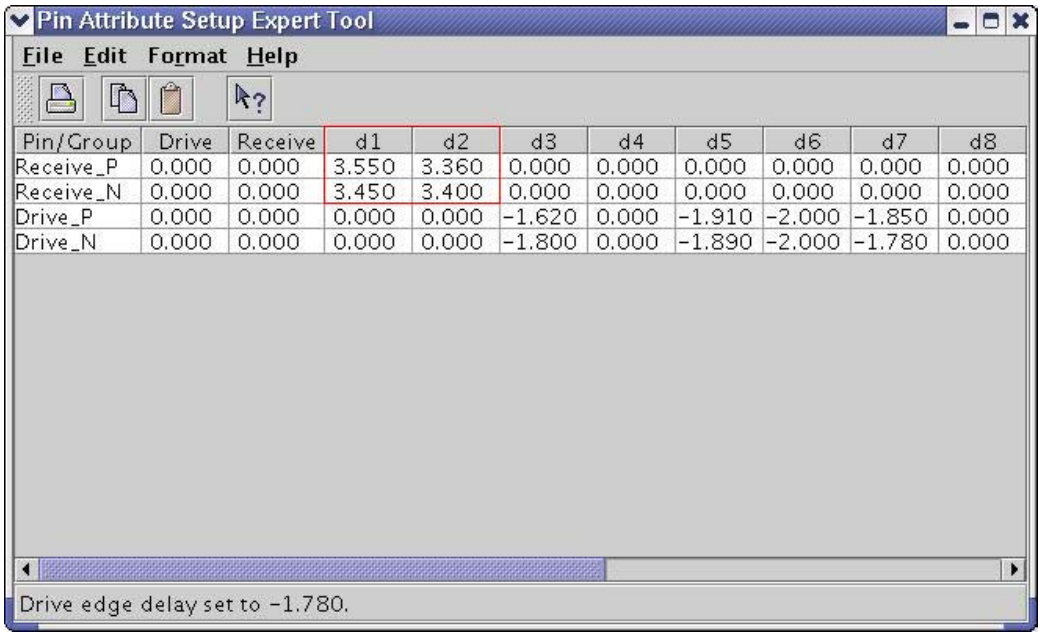


Figure 8: Switch into terminated ATE Rx mode (uncompensated)

The other way around, starting with the unterminated receiver mode, the receiver detects the static 400mV input signal at the beginning. After switching to the terminated receiver mode, the signal is recognized as a 300mV steady voltage as shown in Figure 8. The associated time delay for turning on the termination is 3.55ns.



Pin/Group	Drive	Receive	d1	d2	d3	d4	d5	d6	d7	d8
Receive_P	0.000	0.000	3.550	3.360	0.000	0.000	0.000	0.000	0.000	0.000
Receive_N	0.000	0.000	3.450	3.400	0.000	0.000	0.000	0.000	0.000	0.000
Drive_P	0.000	0.000	0.000	0.000	-1.620	0.000	-1.910	-2.000	-1.850	0.000
Drive_N	0.000	0.000	0.000	0.000	-1.800	0.000	-1.890	-2.000	-1.780	0.000

Figure 9: Edge compensations with cross connection setup

Since the intrinsic delay for switching receiver termination (resulting in drive edges to be shifted earlier in time by entering a negative pin attribute value) is “over-compensated” by round trip ahead of time, the final values to be entered as pin attributes are positive as Figure 9 indicates. The waveforms for termination switching after compensation are shown in Figure 10 and 11.

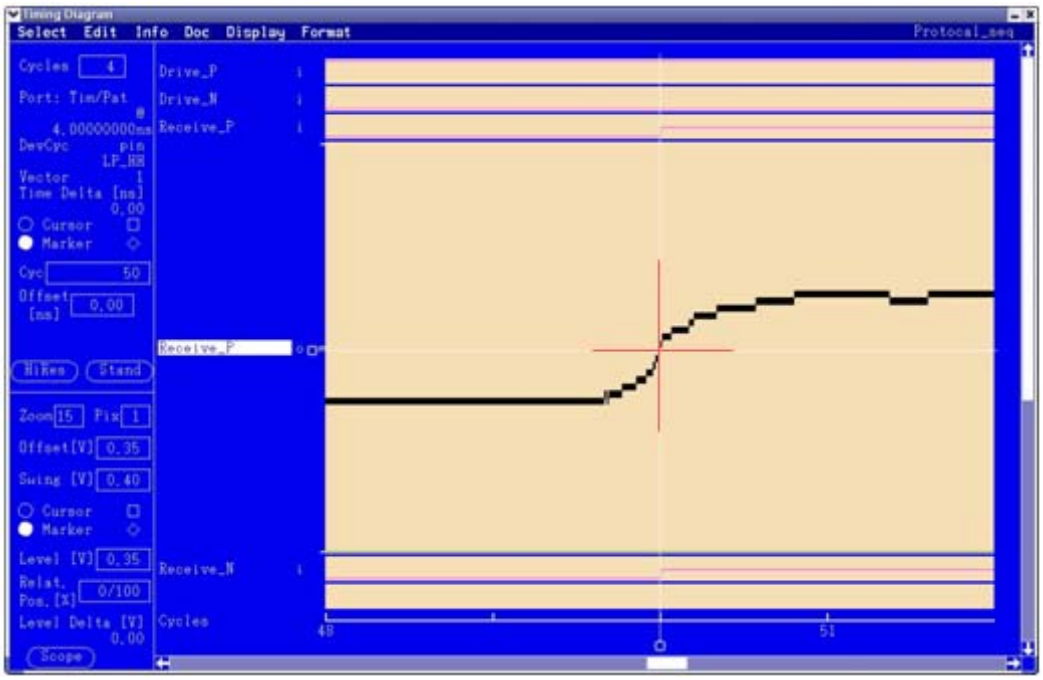


Figure 10: Switch into unterminated ATE Rx mode (compensated)

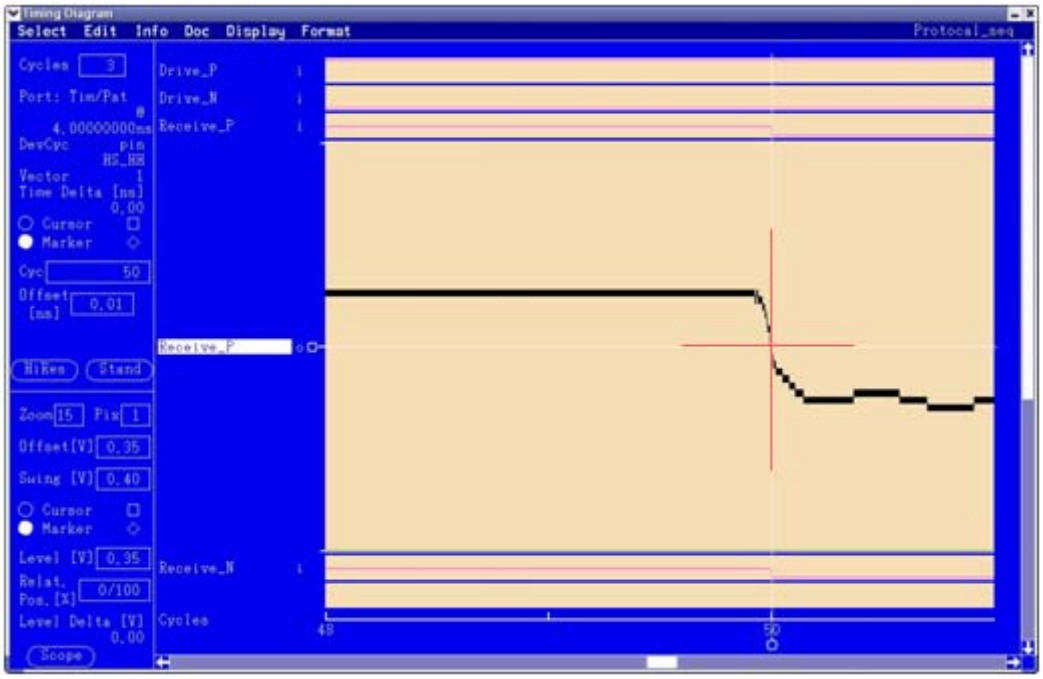


Figure 11: Switch into terminated ATE Rx mode (compensated)

3.2. Receiver channel compensation with customer device setup

When a customer device load board is docked to the tester, the signal transmission path is further extended up to the DUT pin as shown in Figure 12. Therefore, in addition to the system calibration, a fixture delay calibration, which is load board specific, is further needed to cover the trace from the pogo pin to the DUT socket pin. After calibration, the amount of fixture delay $t_{fixture}$ will be stored in the ch_attributes (channel attributes) directory under the device directory, and is taken into consideration by SmarTest whenever the device setup is loaded to ensure the point in time a signal appears at the DUT pin is referred to as the t=0 point.

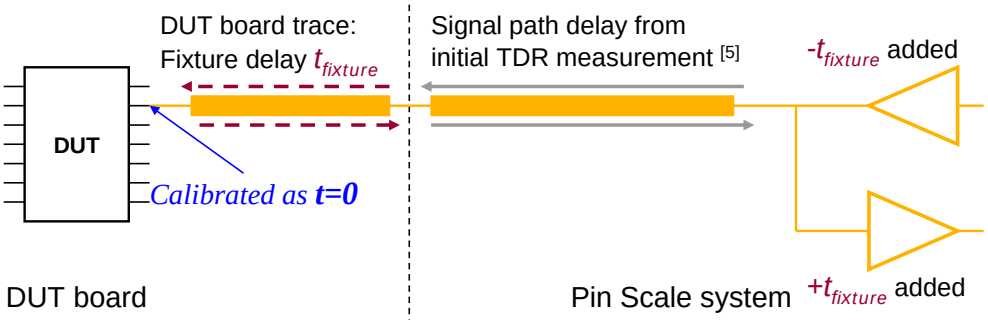


Figure 12: Signal propagation path with a customer device

Unlike the values in the pin attributes file, which are per-pin and per-edge based, the values in the channel attributes file for the fixture delay are specified on a per-pin basis. Hence for each IO pin, the system will apply the same amount of $t_{fixture}$ to both the internal driver and receiver, however, with the opposite timing directions. That means that the internal driver is programmed earlier in time for the drive action, while the receiver is programmed later in time for the compare action. Thus, the timing difference between the internal driver and receiver in adds up to $2*t_{fixture}$.

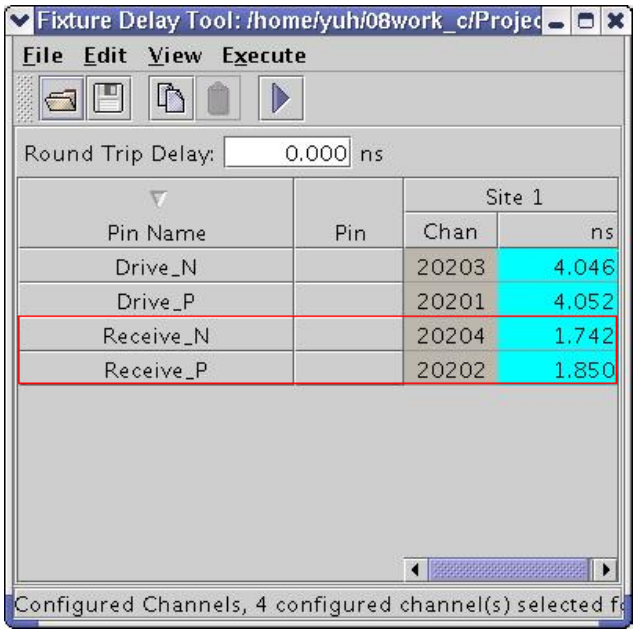


Figure 13: Fixture delay calibration

In this example, the fixture delay for the Receive_P pin (channel 20202) is set to 1.850ns as shown in Figure 13. This matches to the observed waveform shown in Figure 14, for which the compensation data from the previous cross connection setup are taken (neglecting the fixture delay added by the very short traces on the cross connection board). It can be seen that the timing difference on the Receive_P pin is measured to be 3.71ns, which is twice as the fixture delay value in Figure 13.

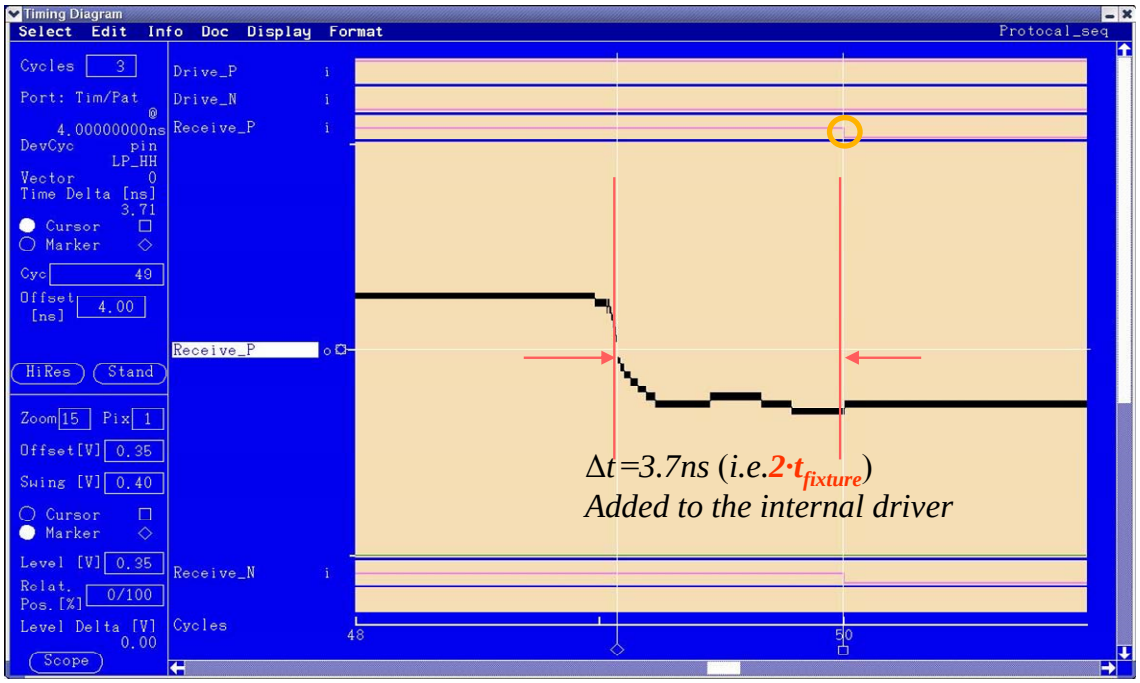


Figure 14: Timing difference raised by the fixture delay

As a result, compared to the original Figure 9, $2*t_{fixture}$ is added to the corresponding channels on top of the compensated drive edges as shown in Figure 15.

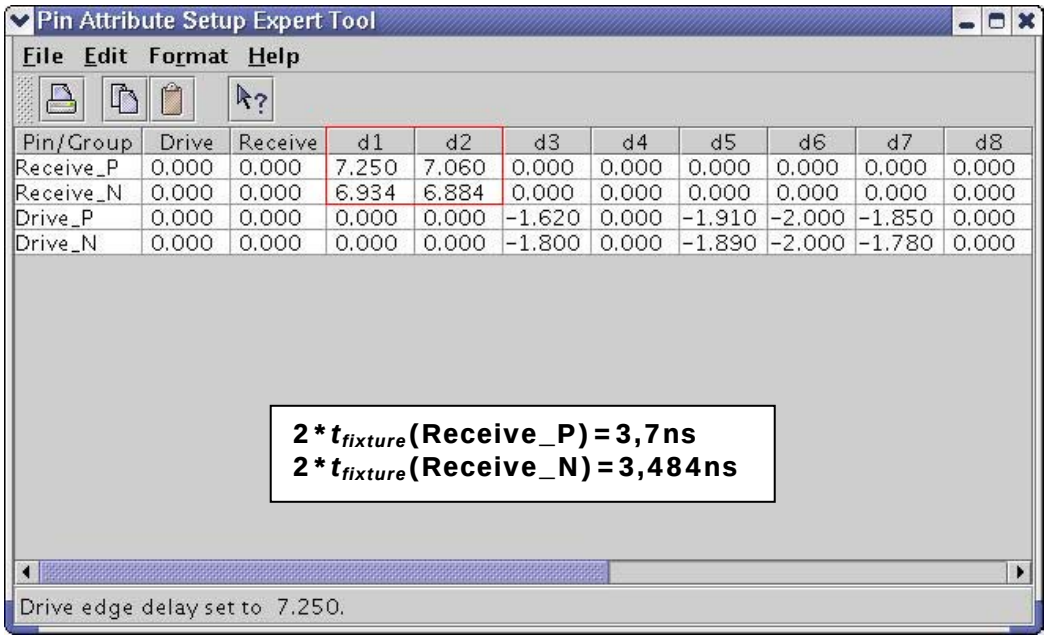


Figure 15: Edge compensations with customer device setup

4. MIPI transition waveform

During normal operation a data lane will be either in Low-Power control mode or High-Speed data transmission mode. Low-Power mode incorporates control states (LP-xx) which are used to lead a Start-of-Transmission sequence or to conclude an End-of-Transmission sequence. The High-Speed data transmission happens always in bursts and starts from, and ends with, a Stop state (LP-11). The lane is only in High-Speed mode during data bursts. The sequence to enter the High-Speed mode is LP-11, LP-01, LP-00, after which the data lane remains in High-Speed mode until another LP-11 is received. Figure 16a shows such a sequence.

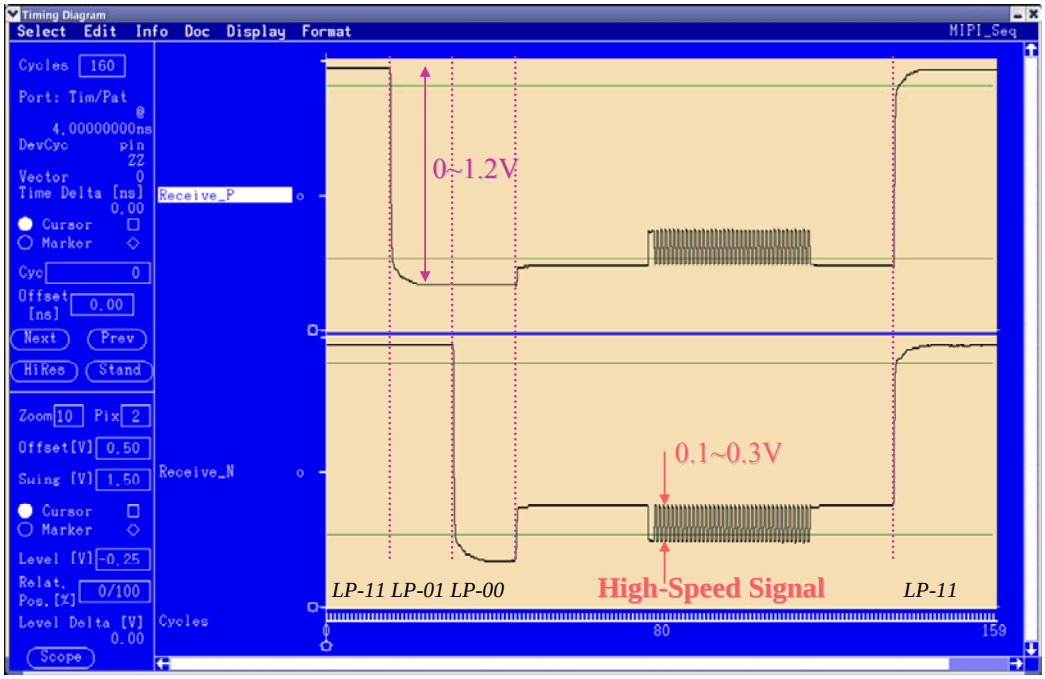


Figure 16a: High-Speed data transmission sequence in timing diagram

Compared with Figure 16b, it can be seen that both High-Speed and Low-Power signals are properly received and interpreted by the ATE with a corresponding receiver mode.

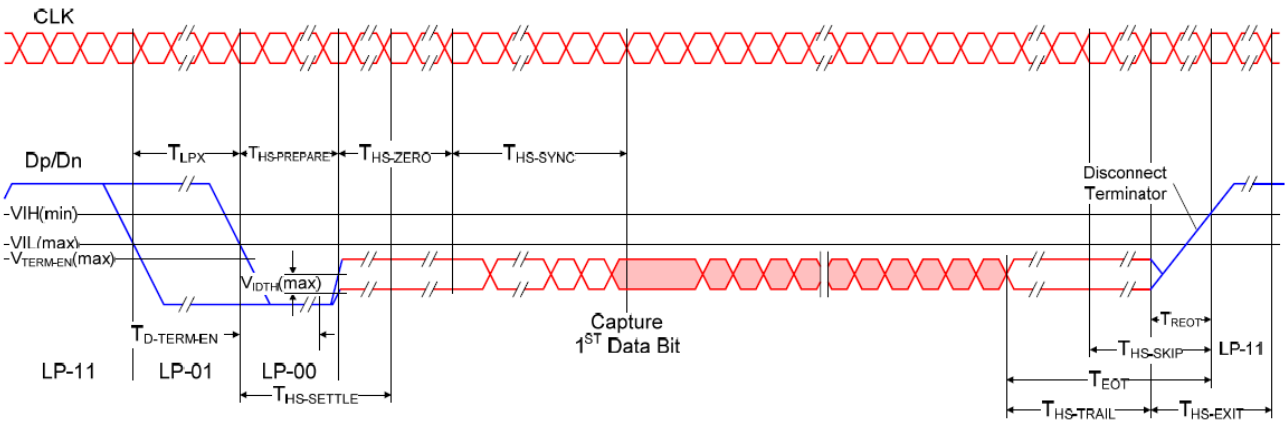


Figure 16b: High-Speed data transmission sequence from MIPI standard [2]

5. Summary

To complete the topic on MIPI D-PHY test, this paper further elaborated the solution for MIPI D-PHY transmitter tests. On top of the source-synchronous nature of data transmission, it is the need to provide flexible tester receiver modes, which makes the DUT transmitter test a non-trivial challenge to normal ATEs:

1. True differential and independent single-ended comparators per differential pin pair
2. Multi-level comparator thresholds
3. Correct signal termination (both terminated and unterminated receiver modes)

Taking these requirements into account, two different approaches were introduced:

1. Separate the High-Speed and Low-Power test and address them in different test suites.
2. Combine both the High-Speed and Low-Power modes to test them within a single pattern.

Two different approaches are possible:

2a) Program the High-Speed signal and Low-Power signal into two separate level sets and change between them with CLEV firmware command. This method enables to switch between differential and single-ended receiver modes and to set up precise compare thresholds but has the disadvantage of certain “blind” cycles for tester receivers during receiver mode switching.

2b) Program both High-Speed and Low-Power signals into the same test suite, and switch between terminated and unterminated receive modes on the fly. Though being a little more complex than approach 2a), this technique makes it possible for the tester receiver to interpret signals without “blind” cycles and to keep track of signal transitions from High-Speed to Low-Power mode and vice versa.

The main focus of this paper is the second approach. By selecting differential pin pairs for receiver pins, the user is able to take advantage of the flexibility provided by Verigy’s Pin Scale cards to form either true differential or independent single-ended comparators. With the adoption of the intermediate compare threshold, the user is able to implement multi-level comparison for both low-swing (~200mV) High-Speed signals and large-swing (~1.2V) Low-Power signals. These compare actions are accompanied with correct signal termination mode on the tester receiver side, which requires special attention, since termination must be changed on the fly within a pattern. However, this can be achieved by combining the tester receive actions with the driver’s data drive and High-Z switching actions while carefully compensating intrinsic delay, round trip delay and fixture delay affecting the timing of such drive actions. To this end,

test engineers have learnt all the subtleties to properly terminate MIPI signals for multi-level waveform detection.

6. Acknowledgements

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