Hideo Okawara's
Mixed Signal Lecture Series

DSP-Based Testing – Fundamentals 20
Effect of Jitters in Sampling Clock and Test Signal

Verigy Japan

December 2009

Preface to the Series

ADC and DAC are the most typical mixed signal devices. In mixed signal testing, analog stimulus signal is generated by an arbitrary waveform generator (AWG) which employs a D/A converter inside, and analog signal is measured by a digitizer or a sampler which employs an A/D converter inside. The stimulus signal is created with mathematical method, and the measured signal is processed with mathematical method, extracting various parameters. It is based on digital signal processing (DSP) so that our test methodologies are often called DSP-based testing.

Test/application engineers in the mixed signal field should have thorough knowledge about DSP-based testing. FFT (Fast Fourier Transform) is the most powerful tool here. This corner will deliver a series of fundamental knowledge of DSP-based testing, especially FFT and its related topics. It will help test/application engineers comprehend what the DSP-based testing is and assorted techniques.

Editor's Note

For other articles in this series, please visit the Verigy web site at www.verigy.com/go/gosemi.

Effect of Jitters in Sampling Clock and Test Signal

Recently more and more ADC and DAC are getting employed in high frequency applications such as telecommunication devices and digital consumer audio/video devices. The signal frequency is getting so high that the converter devices need high quality sampling clocks and test signals. In this issue, let's look at the effect of jitters in the sampling clock and the test signal.

Basics

When you test an n-bit linear ADC for its SNR, if you are familiar with mixed signal test, you may recall the famous equation as follows.[1]

$$SNR[dB] = 6.02 \cdot n + 1.76 \qquad (1)$$

This equation tells the theoretically maximum SNR based on the quantization noise in A to D conversion. In a real device the sampling timing would fluctuate by the device internal noise and sampling clock jitter so that the SNR attainable would be degraded than the maximum value. So the actual measured SNR value defines the ENOB (effective number of bits) as follows.

$$ENOB[bits] = \frac{SNR[dB] - 1.76}{6.02} \qquad (2)$$

This is a performance indicator of the device under test (DUT).

Effect of Random Jitter in the Sampling Clock

Figure 1 shows how the sampling timing fluctuation gives an impact to the A/D sampled data. It is interpreted as noise in addition to the quantization noise so that the SNR attainable gets lower than the maxim based on the quantization theory.

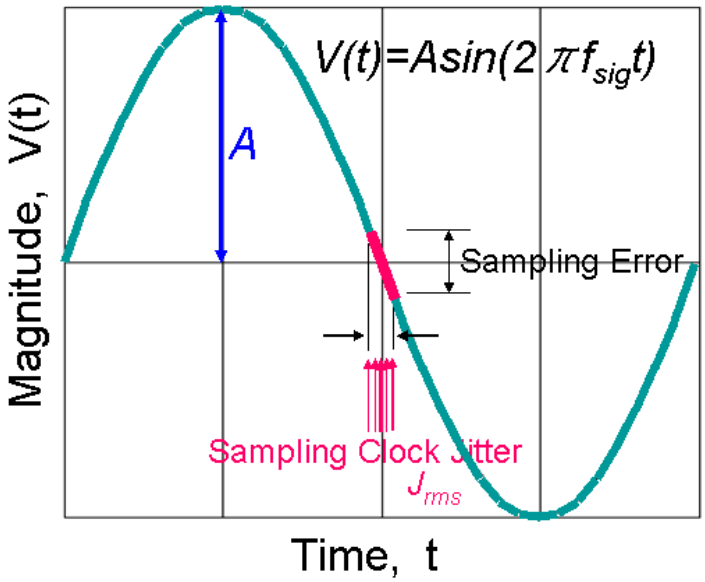

Figure 1: Sampling Clock Jitter Effect

Let's define the input test signal as the sine wave below

$$v(t) = A\sin(2\pi \cdot f_{sig} \cdot t) = A\sin(\omega \cdot t) \qquad (3)$$

A : the test signal amplitude
fsig : the test signal frequency

Differentiating the sine wave goes as below

[1] You can find how to derive the equation in the first newsletter article of this lecture series "DSP-Based Testing – Fundamentals."

$$\frac{dv}{dt} = A\omega \cdot \cos(\omega \cdot t) \tag{4}$$

So when the sampling clock jitter is Δt, it generates the noise of Δv, which is described as below.

$$\Delta v = A\omega \cdot \cos(\omega \cdot t) \cdot \Delta t \tag{5}$$

The RMS of the cosine in (5) is 1/sqrt(2) so that the RMS noise of Δv can be described by the clock jitter Δv(rms)= Jrms as below.

$$\Delta v(rms) = \frac{A\omega}{\sqrt{2}} \cdot J_{rms} \tag{6}$$

Considering the RMS of the test signal as A/sqrt(2), the SNR can be described as follows.

$$\begin{aligned} SNR[dB] &= 20\log\left(\frac{RMS\_Signal}{RMS\_Noise}\right) = 20\log\left(\frac{\frac{A}{\sqrt{2}}}{\frac{A\omega}{\sqrt{2}} J_{rms}}\right) \\ &= 20\log\left(\frac{1}{\omega \cdot J_{rms}}\right) = 20\log\left(\frac{1}{2\pi \cdot f_{sig} \cdot J_{rms}}\right) \end{aligned} \tag{7}$$

The point of Equation (7) is the influence of jitter depends on the test signal frequency. The sampling rate has nothing to do with it. This is so important that you should keep it in mind.

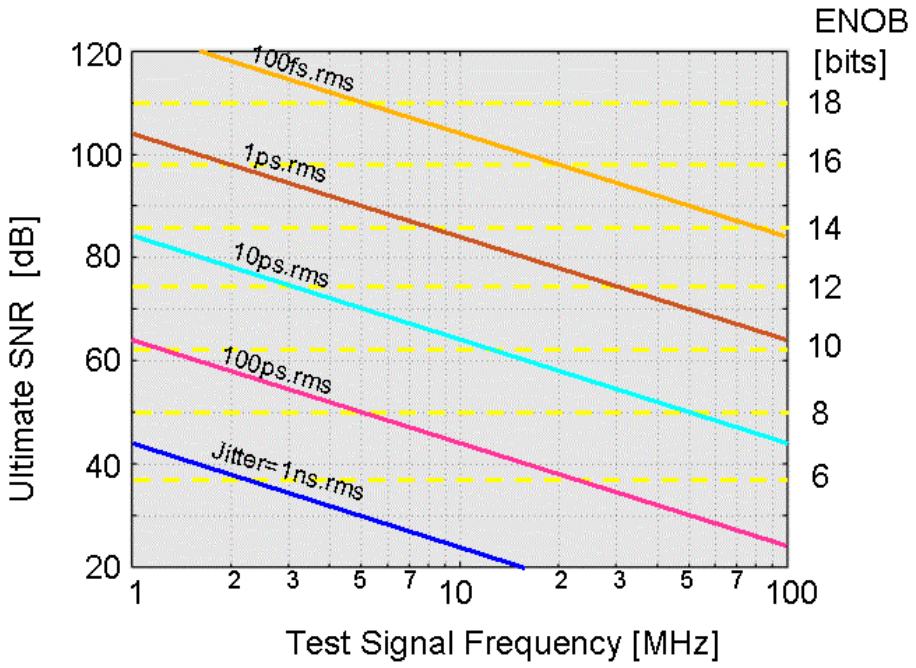

Figure 2: SNR and ENOB vs. Sampling Clock Jitter

Figure 2 is a graphical expression of Equation (7). When you are informed about the test signal frequency and the ENOB of a DUT ADC, you should promptly figure out the required jitter performance for the sampling clock according to Figure 2. For instance, when you need to test an ADC with 30MHz and 12 bits of ENOB, the sampling clock must have better performance than 1ps.rms of jitter.

Figure 3 demonstrates how the sampling clock jitter influences the ADC spectrum appearance. This is a simulation of 14-bit ADC so that the ultimate SNR is 86dB. The noise floor based on the quantization noise is colored red in the graph. The sampling rate is 102.4Msps and the test signal frequency is 20.3MHz. If the sampling clock contains 10ps.rms of random jitter, the noise floor is raised as blue line so that the SNR degrades to 58dB. Then ENOB is deteriorated to 9.3 bits. (See Figure 2)

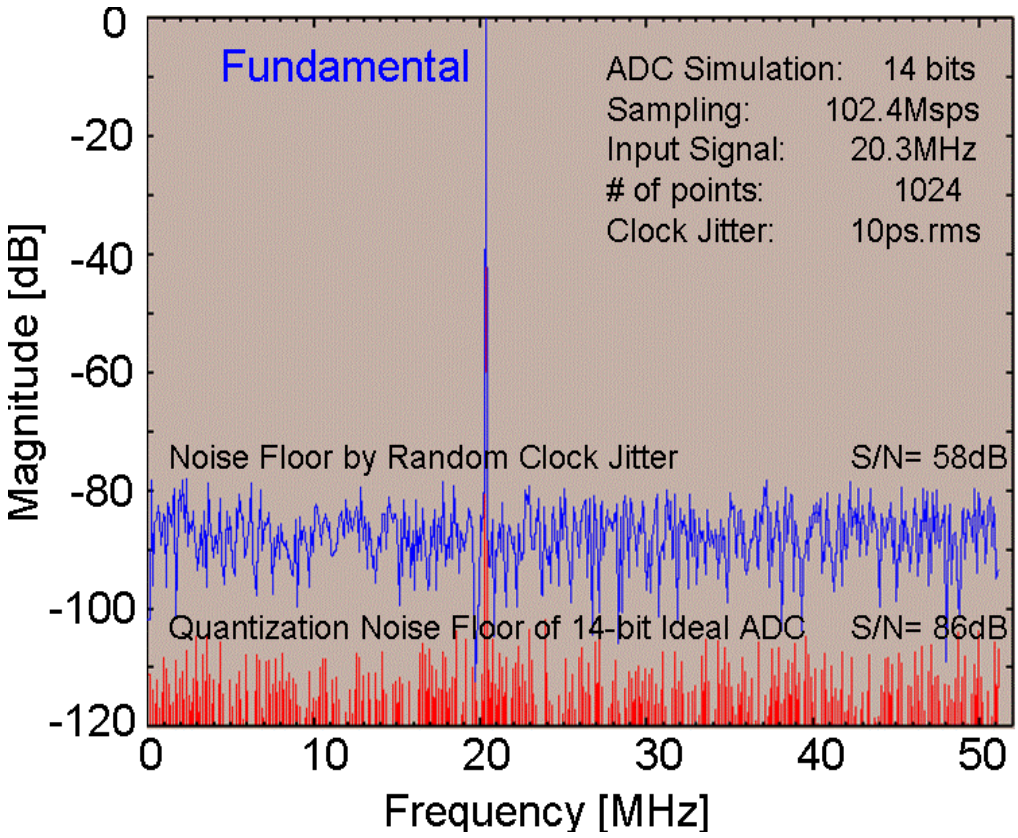

Figure 3: Spectrum when ADC clock contains random jitter

Effect of Deterministic Jitter in the Sampling Clock

As discussed in the previous section, when the sampling clock contains random jitter, it appears as raising the noise floor in the frequency spectrum. If the clock contains deterministic jitter, how does it appear in the frequency spectrum?

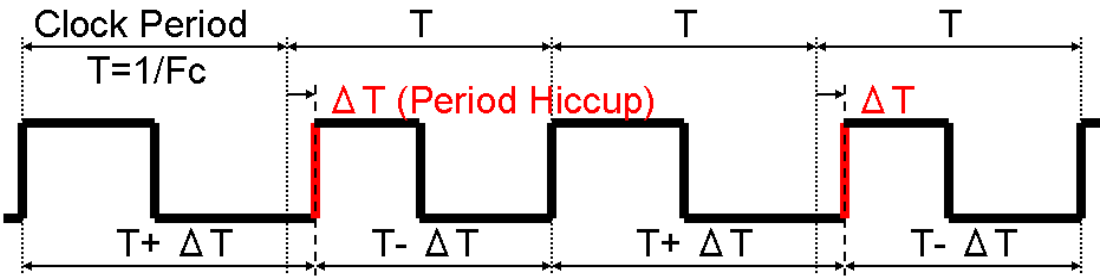

Figure 4: Irregular sampling clock (Hiccup Jitter)

Look at Figure 4. It depicts a clock stream whose frequency is *Fc*. The rising edges shift ΔT every two pulses so that the period *T* (=1/*Fc*) is irregular as hiccup. This becomes deterministic jitter. This kind of situation could occur when multiple pin-driver edges are assigned to realize a higher clock frequency. This operation may be called X-mode. Figure 5 depicts the frequency spectrum of the clock containing such hiccup jitter, which generates spurious components colored red in the figure.

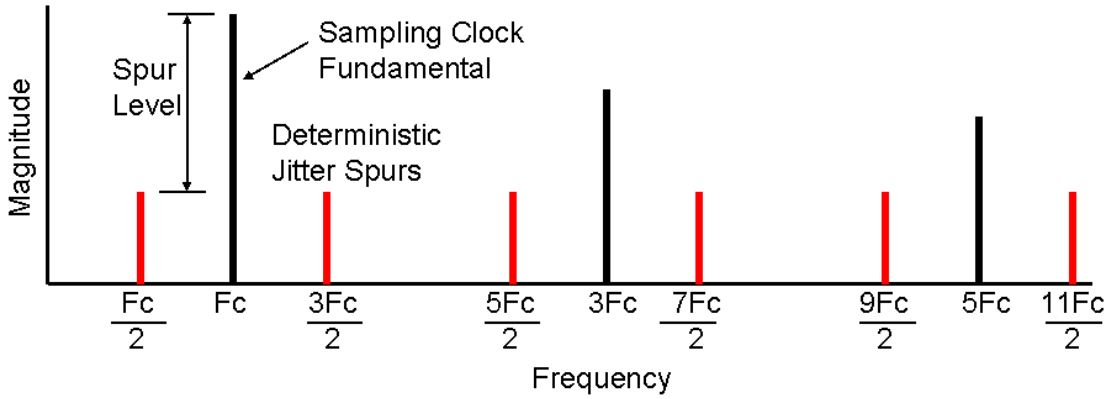

Figure 5: Spectrum of irregular clock

If the sampling clock has this kind of irregularity, how would the ADC capture a test signal? See Figure 6. (a) The fundamental sampling clock (*Fc*) generates a normal spectrum in the Nyquist plane. (b) The irregular shifts in every two pulses can look as *Fc*/2 clock so that the spurious spectrum appears as red. (c) Consequently the irregular hiccup generates the virtual spurious spectrum in the Nyquist plane. This phantom is always located symmetrically to the fundamental spectrum. When the test signal frequency is *Ft*, the spur appears at (*Fc*/2)-*Ft*.

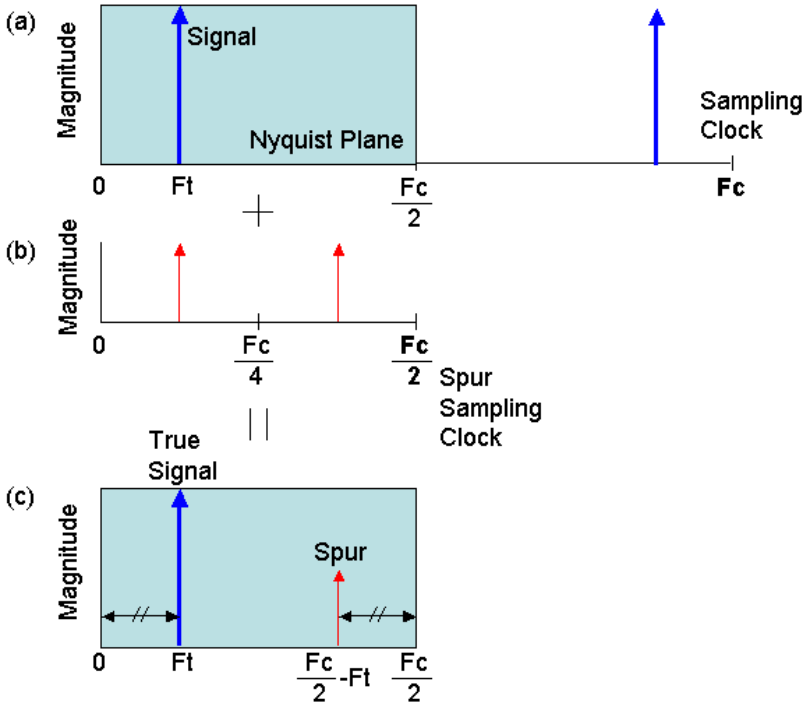

Figure 6: Mechanism of virtual spur

If you would observe a strange image spurious at (Fc/2)-Ft as Figure 6(c), you should investigate the sampling clock integrity.

Figure 7 shows the simulation of the hiccup jitter effect. The 14-bit ADC runs at the rate of 102.4Msps that contains 10ps hiccup shift of clock edge as Figure 4 along with 10ps.rms random jitter. The random jitter in the clock raises the noise floor, and the deterministic jitter generates the phantom spur at the symmetrical location to the signal.

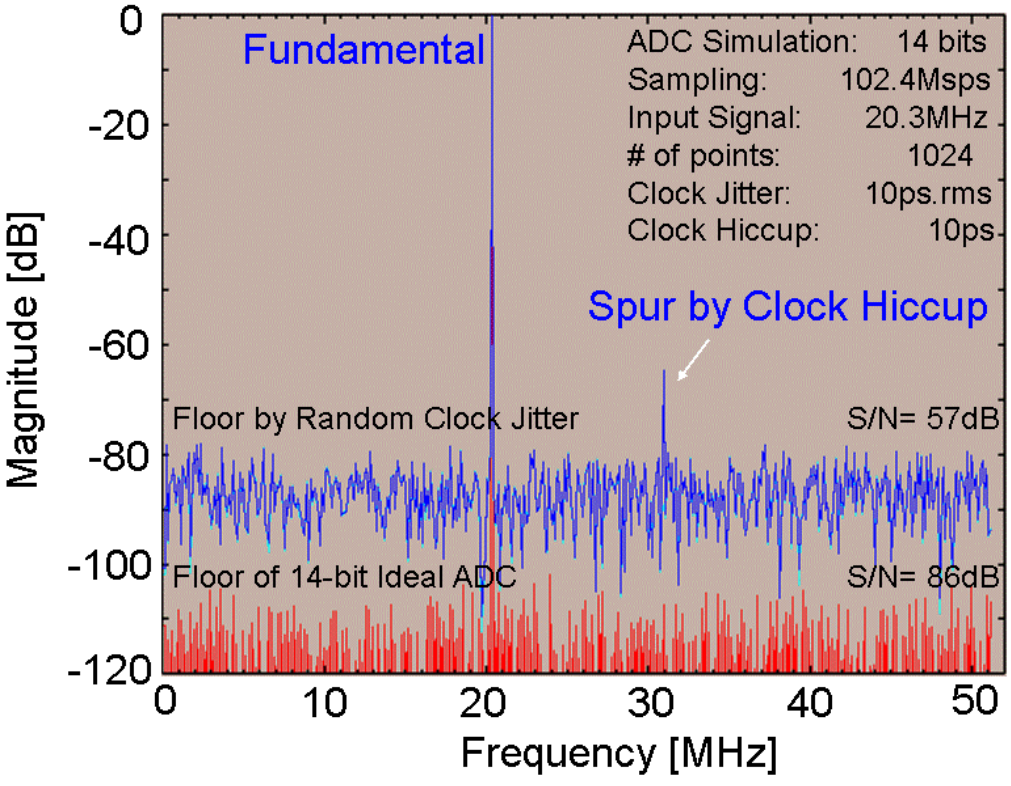

Figure 7: Effect of Deterministic Jitter + Random Jitter

Effect of Jitter in the Test Signal

When the test signal contains a jitter, the situation is the same as the case of sampling clock. The jitter in the test signal is usually discussed as the residual phase noise. Figure 8 depicts the sinusoidal waveform containing a phase noise. When the test signal is sampled with an ideal sampling clock, the sampled data would contain voltage errors or noise. Let's estimate the SNR degradation by the noise.

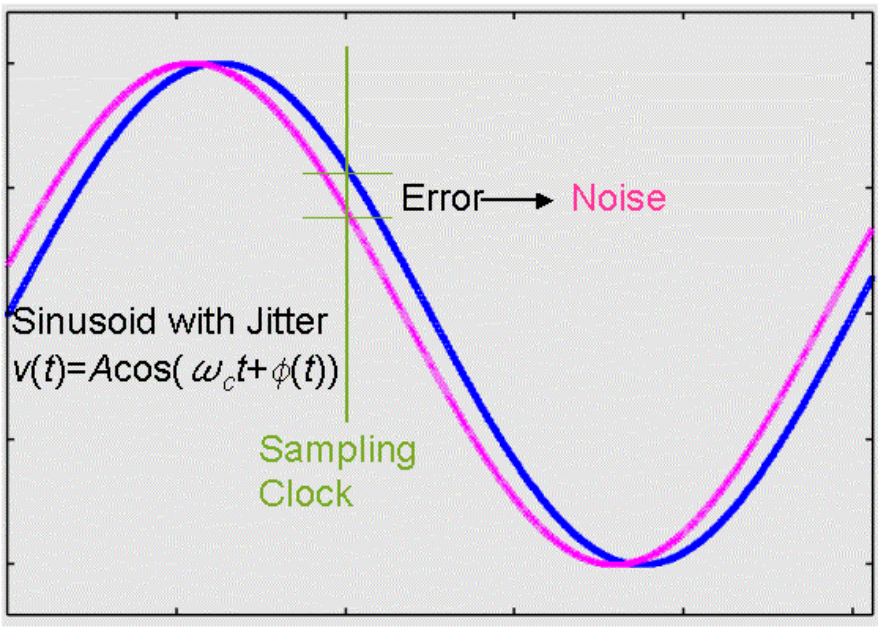

Figure 8: Test Signal Jitter

The test signal containing phase noise can be described as follows.

$$\begin{aligned} v(t) &= A\cos\left(\omega_c t + \phi(t)\right) \\ &= A\cos\phi(t)\cdot\cos\left(\omega_c t\right) - A\sin\phi(t)\cdot\sin\left(\omega_c t\right) \end{aligned} \tag{8}$$

where ω_c is the test signal angular frequency, and $\phi(t)$ is the residual phase noise, which is very small and almost zero so that Equation (8) can be approximated as follows.

$$\begin{aligned} v(t) &= A\cos\left(\omega_c t\right) - \phi(t)A\sin\left(\omega_c t\right) \\ &= A\cos\left(\omega_c t\right) - \phi_a\cos\left(\omega_a t\right)\cdot A\sin\left(\omega_c t\right) \end{aligned} \tag{9}$$

where the phase noise $\phi(t)$ is represented as a sinusoid.

The first term is the true test signal, and the second term is the noise. So the signal to noise ratio (SNR) can be described as follows.

$$SNR = \frac{SignalPower}{NoisePower} = \frac{\frac{A^2}{2}}{\frac{A^2}{2}\frac{\phi_a{}^2}{2}} = \frac{2}{\phi_a{}^2} \tag{10}$$

$$SNR[dB] = 10\log\frac{2}{\phi_a{}^2} \tag{11}$$

The phase noise amplitude ϕ_a [rad] can be converted into the time fluctuation by dividing 2 πf_{sig}. If the RMS magnitude of the phase noise jitter is denoted as Jp_{rms} [sec.rms], the jitter amplitude Jpk [sec] can be described as follows.

$$J_{pk} = \sqrt{2}Jp_{rms} = \frac{\phi_a}{2\pi f_{sig}} \tag{12}$$

Then ϕ_a can be described as follow.

$$\phi_a = 2\pi \cdot f_{sig}\sqrt{2}Jp_{rms} \tag{13}$$

Applying Equation (13) into Equation (11), it can be described as follow.

$$\begin{aligned} SNR[dB] &= 10\log\frac{2}{\left(2\pi \cdot f_{sig}\sqrt{2}Jp_{rms}\right)^2} \\ &= 10\log\frac{1}{\left(2\pi \cdot f_{sig}Jp_{rms}\right)^2} \\ &= 20\log\left(\frac{1}{2\pi \cdot f_{sig}Jp_{rms}}\right) \end{aligned} \tag{14}$$

Actually this is very similar to Equation (7) so that the effect can be presented in the same graph as Figure 2. In the case of random clock jitter, the effect appears as the raised noise floor. However phase noise of the test signal is a kind of phase modulation, the effect would appear as the residual side lobe in the vicinity of the fundamental tone.