Hideo Okawara's
Mixed Signal Lecture Series

DSP-Based Testing – Fundamentals 37
F-matrix Simulation TDR

Verigy Japan
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Preface to the Series

ADC and DAC are the most typical mixed signal devices. In mixed signal testing, analog stimulus signal is generated by an arbitrary waveform generator (AWG) which employs a D/A converter inside, and analog signal is measured by a digitizer or a sampler which employs an A/D converter inside. The stimulus signal is created with mathematical method, and the measured signal is processed with mathematical method, extracting various parameters. It is based on digital signal processing (DSP) so that our test methodologies are often called DSP-based testing.

Test/application engineers in the mixed signal field should have thorough knowledge about DSP-based testing. FFT (Fast Fourier Transform) is the most powerful tool here. This corner will deliver a series of fundamental knowledge of DSP-based testing, especially FFT and its related topics. It will help test/application engineers comprehend what the DSP-based testing is and assorted techniques.

Editor's Note

For other articles in this series, please visit the Verigy web site at www.verigy.com/go/gosemi.

Preface

For quality test, an LSI tester must deliver the right signal to the device-under-test (DUT), requiring the tester's pin driver to overcome the capacitance of the DUT input terminal. Although input capacitance is usually specified in the device specifications, it typically is not measured because the LSI tester is not equipped with the right instruments. The purpose of this report, and the research behind it, is to measure LCR on a device input using a waveform sampler.

The basic methodology is a traditional time-domain reflectometry (TDR) utilizing a clock supplied by a regular pin driver as the test signal. The signal path to the DUT is then monitored by connecting a simple resistive probe.

This month article introduces the simulation result performed using the four-terminal matrix method introduced in the previous issue[1], which is simple and primitive but good enough for predicting distinctive waveforms on a transmission line. The actual measurement results will be reported in the next month issue.

Principle

The principle of TDR is based on signal reflection at the terminal of a transmission line as Figure 1 illustrates. When an incident signal is asserted on to a transmission line, it travels toward the end of the line. If the line is well terminated with the characteristic impedance (*Zo*) of the line, the entire incident signal energy is absorbed in the termination impedance so that no reflection occurs. If the terminal is not well terminated, part of the energy is reflected and travels back toward the input port. The ultimate condition is when the line is terminated with an "open" or "short". When the output port is left "open," the incoming signal is reflected 100% with the same polarity. When the output port is "short-circuited", the incoming signal is reflected 100% with the polarity inverted. If you observe the signal somewhere on the way of the transmission line, you can see the composite signal of the incident and the delayed reflected signals. Therefore by analyzing the reflected waveform, you can estimate what the termination impedance would be. This is the principle of the TDR.

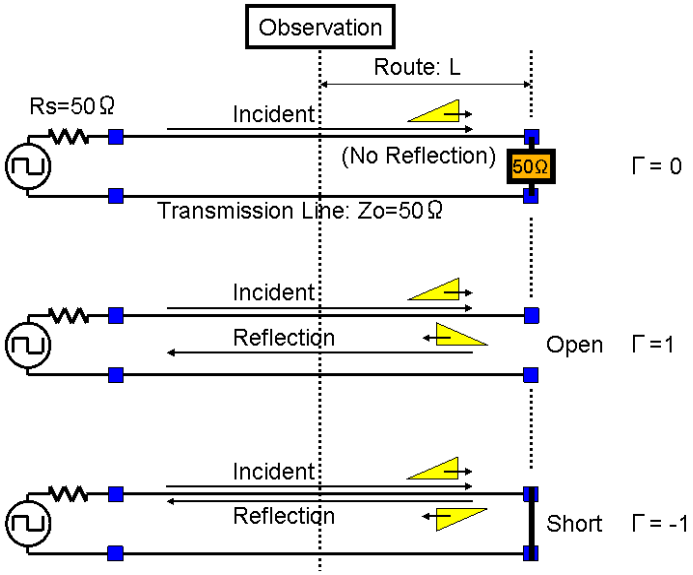

Figure 1: Reflection of Signal

[1] Mixed Signal Lecture Series "DSP-Based Testing – Fundamentals 35 F-matrix Simulation"

Composite Signal Waveform

Figure 2 depicts how the composite signal waveform looks at the observation point when the terminal is terminated with "open" and "short". The delay of the reflected signal equals the time necessary for the signal to travel twice the electrical length of "L" in Figure 1.

The point is the polarity of the reflected signal. When "open," the reflection signal has the same polarity to the incident signal. When "short," the reflection has the opposite polarity to the incident. "Open" associates with capacitive load, while "short" associates with inductive load.

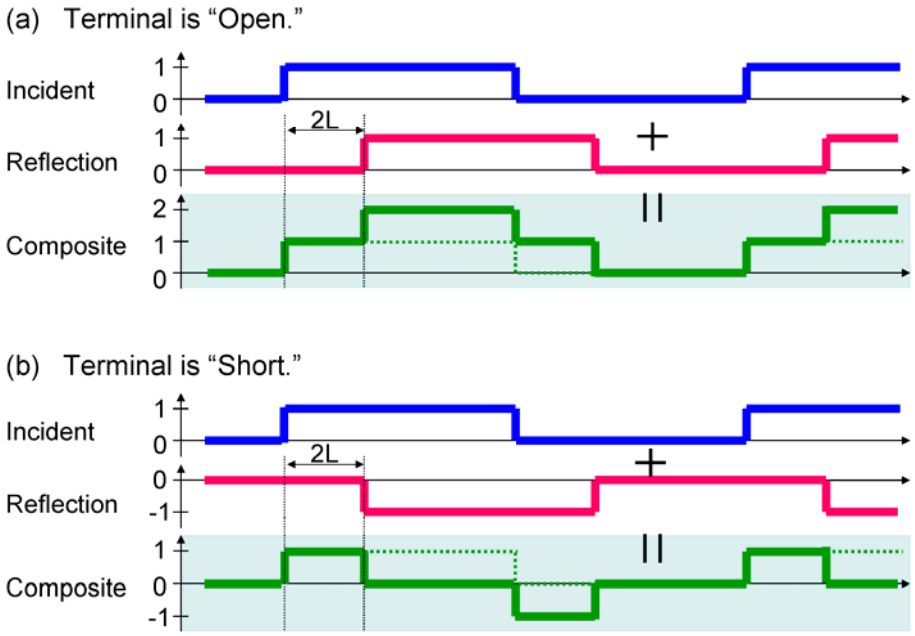

Figure 2: Reflection of Signal

Test Configuration

Figure 3 illustrates a schematic of the experimental setup. The 50[Ω] transmission line may be micro-strip lines on a DUT board. Coaxial cables are used in the experiment that will be reported next month.

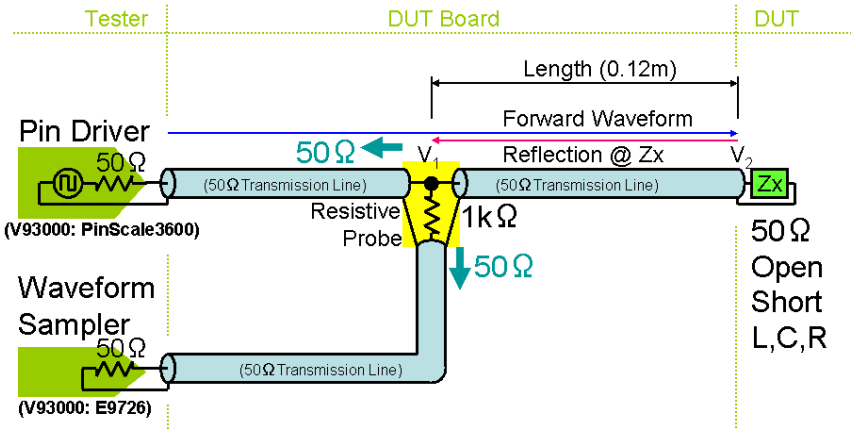

Figure 3 Experimental Circuit Diagram

To pick up the signal with minimum interference, the transmission line needs to be sensed with a high impedance condition. One of the most simple and typical techniques for high impedance sensing is a passive resistive probe. As shown in Figure 4, the signal at the probing point is sensed with a 1[kΩ] resistor, and the other end of the resistor is connected to the 50[Ω]-transmission line. The transmission line is terminated with 50[Ω] that is the input impedance of the sampler. So the terminated transmission line can be seen as a 50[Ω]. Consequently the probing point is sensed with 1050[Ω] so that the probe can pick up the signal with little effect. The sensed signal is divided by 50/1050 so that the signal level introduced to the sampler is reduced by approximately 26[dB].

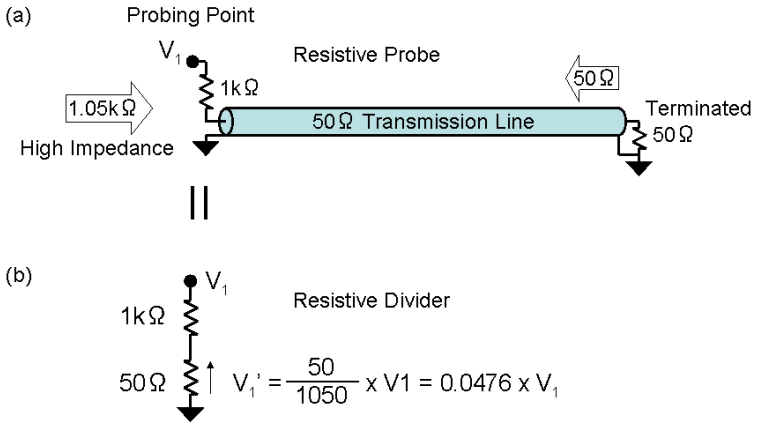

Figure 4 Resistive Probe

The other end of the 1[kΩ] resistor is guided to a waveform sampler for waveform analyses. A digital pin driver drives a clock signal and a waveform sampler captures the composite signal waveform.

Simulation Model

Figure 5 is a model of the transmission line from the probing point (V_1) to the DUT input (V_2) shown in Figure 3. The signal path from the pin driver to the probing point is simplified as the signal source V_0 with a source impedance of Rs=50[Ω]. The resistive probe is supposed to be very high impedance and give no effect to the probing point.

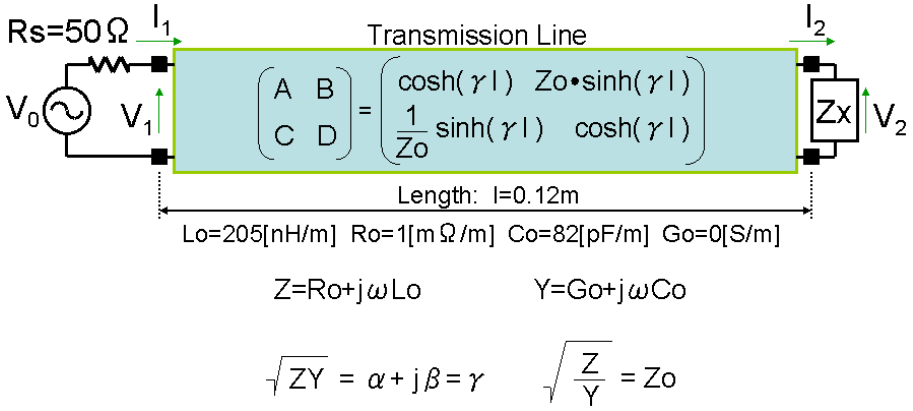

Figure 5 Transmission Line Model

Co, *Lo*, *Ro* and *Go* are characteristic parameters per unit length of the transmission line. A typical *Co* is 82[pF/m] for a coaxial cable. The characteristic impedance *Zo* is 50[Ω] so that *Lo* is estimated

as 205[nH/m]. Figure 5 includes the F-matrix model of the transmission line. *Ro* is set 1[mΩ/m] and *Go* is set zero for simplicity.

The relationship between V_1 and V_2 can be described with using the F-matrix as follows:

$$\begin{pmatrix} V_1 \\ I_1 \end{pmatrix} = \begin{pmatrix} A & B \\ C & D \end{pmatrix} \begin{pmatrix} V_2 \\ I_2 \end{pmatrix} \quad (1)$$

$$V_2 = I_2 \cdot Zx \quad (2)$$

$$V_0 = I_1 \cdot Rs + V_1 \quad (3)$$

Then the signal V_1 can be resolved as follows:

$$V_1 = \frac{A \cdot Zx + B}{Rs \cdot (C \cdot Zx + D) + (A \cdot Zx + B)} \cdot V_0 \quad (4)$$

The resistive probe senses the signal V_1 with a series network of 1[kΩ] and 50[Ω]-terminated transmission line so that the actual signal conveyed to the sampler would be attenuated by approximately 26 dB. However, the absolute level of the signal is not essential in this discussion. The waveform of the reflected signal should precisely be analyzed.

According to Equation (4), when waveform V_0 is given, waveform V_1 can be simulated with the FFT (Fast Fourier Transform) and IFFT (Inverse FFT) signal processing methods depicted in Figure 6. The input waveform V_0 is FFT'd and decomposed into frequency components. Each component is then processed with Equation (4). The summation of those components is then IFFT'd to reconstruct the output waveform V_1. This is a classic and primitive signal processing procedure. FFT and IFFT are essential data processing in mixed signal testers. Consequently, the F-matrix method is handy in analyzing simple passive circuits in this experiment.

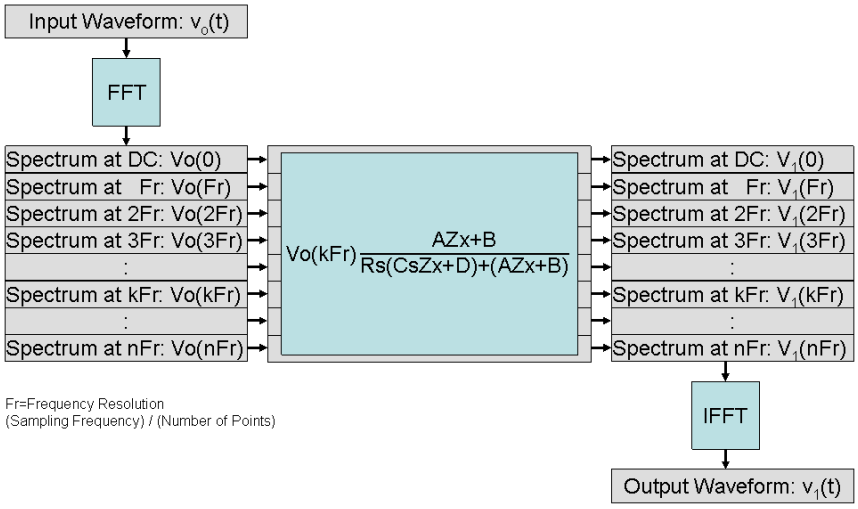

Figure 6 Data Processing Procedure of Simulation

Simulation Result

The most typical conditions - "open," "50[Ω]" and "short" - are simulated using the signal processing method discussed in the previous section. Figure 7 shows the simulated waveforms.

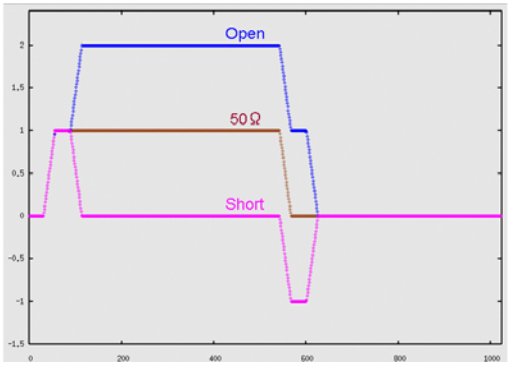

Figure 7 Open/50[Ω]/Short

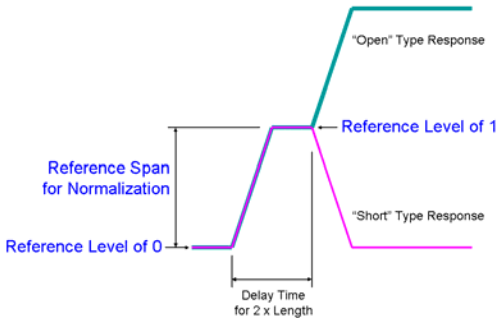

Figure 8 Front Porch of Waveform

The parameters of the clock signal V_0 applied in the simulation is as follows:

Clock Frequency: 50[MHz]

Clock Level: 0[V].. 2[V]

The virtual sampling conditions are as follows:

Number of Samples: 1024 points

Virtual Sampling Rate: 51.2[Gsps]

When *Zx* is 50[Ω], no reflection occurs at *Zx*. Then the composite waveform shows the incident clock waveform (the brown line in Figure 7) and creates a trapezoidal shape. The rising and falling slopes imitate a realistic slew rate of the clock waveform.

The simulated waveforms for "open" and "short" agree with the conceptual pictures in Figure 2. Since the clock frequency is 50[MHz], the duration of the high level is approximately 10[ns]. Each waveform is symmetric with respect to a point, but the left half is enough for analysis. At the rising edge, there is approximately a 1[ns] small step in the open/short reflections. This corresponds to the time necessary for the signal to travel from the probing point to the *Zx* location and to return from the terminal to the probing point. The duration of this porch corresponds to twice the physical distance of 0.12[m] which is the length from the probing point to the terminal in Figure 3.

This small step is particularly useful in the waveform analysis because it indicates the start of the reflection signal and the amplitude reference. In an actual measurement, probably you cannot connect any standard at the terminal which is actually in the device socket. So the "50Ω" response and the "short" response most likely cannot be acquired. Therefore, the resistive probe should be provided at an appropriate distance, such as 0.12[m] in this case, away from the terminal for making the good front porch.

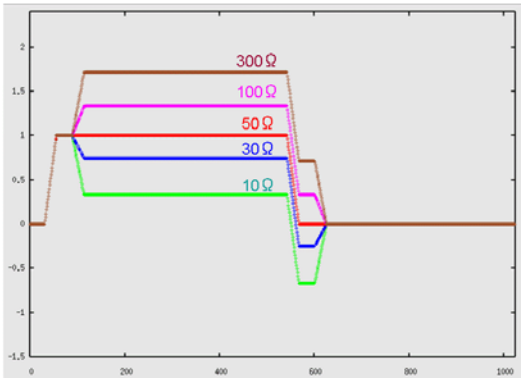

Figure 9 Resistance

Let's look at the simulation results. When *Zx* is a resistance (*R*), Figure 9 shows the simulated response. You can analyze the levels of the horizontal flat lines and estimate the resistance value.

When *Zx* is a capacitance (*C*) and an inductance (*L*), Figures 10 and 11 show the simulated responses respectively. The less capacitance is connected, the more the response assimilates to "open." The less inductance is connected, the more the response assimilates to "short." The very characteristic features are the exponentially rising curves for the capacitances and the exponentially falling curves for the inductances. By analyzing the exponential trends mathematically, you can estimate the capacitance and the inductance values respectively. Actual experimental results will be introduced in the next month article.

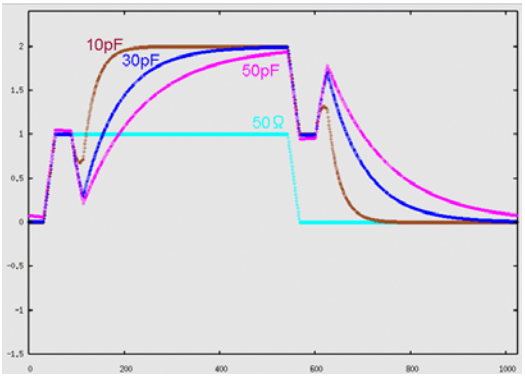

Figure 10 Capacitance

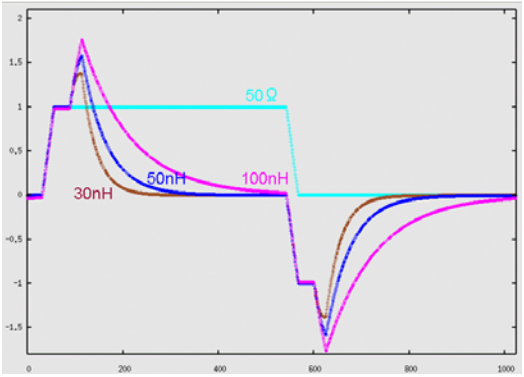

Figure 11 Inductance