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16 Gbps 4-PAM Signal Generation for Real-Time Testing of Multi-Level Signal Receivers

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Abstract

This article proposes a method for testing a device with multi-level signal interfaces. This method utilizes multi-level drivers that generate multi-level signals. The multi-level drivers can test the voltage noise tolerance and the jitter tolerance of a receiver device with multi-level signal interfaces. Experimental results are discussed with a prototype circuit that demonstrates the proposed concept applied to a 16 Gbps 4-PAM Test System.

1. Introduction

Recently, many studies of the multi-level signal transmission method such as pulse amplitude modulation (PAM) technique have been published [1, 2], and all of them shows that the PAM interfaces are promised techniques for improving the transmission rate. Currently, PAM is mainly applied to long-distance transmissions such as Ethernet. However, we believe that with the demand for a higher-speed transmission rate, the PAM technique will be expanded for short distance transmissions such as inter-module and chip-to-chip transmissions.

In order to put the multi-level signal interfaces to practical use for mass production, cost reduction of the multi-level signal interfaces is essential. This means that a cost reduction for testing is also indispensable.

A conventional multi-level signal testing method samples the multi-level signal under test with an A/D converter and analyzes the sampled waveform by digital signal processing (DSP) techniques afterward. For example, the compliance test of Ethernet [3] provides an analysis method of a transmitter output signal waveform by using a high-speed digital real-time oscilloscope. Such a DSP analysis method has a problem in that the analysis time is very long. Consequently, the conventional method can be applied only to devices with smaller number of interfaces, but cannot be applied to devices with a great number of interfaces.

On the other hand, ATE vendors supply digital modules for testing high-speed serial interfaces in real-time. Even though, many studies of high-speed interface testing methods have been conducted [4-6], these methods are developed only for testing binary signal. No real-time testing solution for the multi-level signals has been released at this time.

Our mission is to develop a low-cost testing solution for the multi-level signal interfaces that will be available in advance of anticipated need for mass production. In this article, we propose a real-time functional testing technique for multi-level signal interfaces, especially multi-level signal generation technique for testing receiver devices.

The rest of the article is organized as follows. Section 2 describes the multi-level signal receiver testing and the conventional test system. Section 3 presents a concept of the proposed test system. Section 4 provides experimental results with a prototype circuit to demonstrate the proposed concept. Finally, Section 5 summarizes the article.

2. Multi-Level Signal Receiver Testing and the Conventional Test System

2.1 Challenges for Testing of Multi-Level Signal Receiver

Table 1 shows typical test items for receiver (Rx) devices. Among all those test items, the functional testing is most critical in the production test stage. In order to ensure the reliability of the Rx device under test (DUT), it is important to test the correct functionality of the DUT against voltage variation (voltage noise) and time variation (jitter) in the input signals to the Rx device. Hence, voltage noise tolerance testing and jitter tolerance testing are particularly important.

Table 1: Test Items for Receiver Devices.

Test Item	Description	Priority in Production Test
Functional Testing	Testing the functionality of the DUT	High
Voltage Noise Tolerance Testing	Testing the functionality on the condition that the input signals have a predetermined voltage level variation	High
Jitter Tolerance Testing	Testing the functionality on the condition that the input signals have a predetermined timing jitter	High
Eye Tolerance Testing	Testing the functionality on the condition that the eye of the input signals closes to a predetermined eye opening	Middle
Skew Tolerance Testing	Testing the functionality on the condition that the input signals have a skew between each other	Middle
Common Mode Voltage Tolerance Testing	Testing the functionality on the condition that the input differential signals have a predetermined common mode voltage level	Middle
Input Sensitivity Measurement	Measuring the minimum input amplitude level at which the DUT works correctly	Low
Input Impedance Measurement	Measuring the input impedances of the receivers	Low

Voltage Noise Tolerance Testing: This tests the tolerance for a variation of voltage levels in the input signals to an Rx device. Testing the tolerance of the *multi-level* Rx device against the input voltage level variation requires multi-level voltage drivers that can generate the plural output voltage levels specified independently and that can vary them between the upper and lower limit values in each allowable input voltage range.

The input voltage levels of the DUT are generally specified by a voltage range between the upper and lower limits (Figure 1). In the case of binary signal, when the input voltage level is close to the reference threshold level V_T of the Rx, that is, the input High voltage level becomes the lower limit value $V_{IH,min}$ and the input Low voltage level becomes the upper limit value $V_{IL,max}$, the probability of bit errors becomes high (Figure 1(a)). Therefore, for the binary signal, input voltage margin testing was performed, instead of testing the input voltage noise tolerance by setting the input voltage amplitude to the minimum value ($V_{IL,max}$ to $V_{IH,min}$). Just like the binary signal, the probability of error in the multi-level signals also becomes high when the input voltage levels V_{Ik} (k = 0, 1, …, N-1) are close to the reference threshold levels V_{Tj} (j = 0, 1, …, N-2) of the multi-level Rx (Figure 1(b)). Thus, when testing the input voltage margin of the multi-level signal, the plural input voltage level V_{Ik} must be set to both the upper limit value ($V_{Ik,max}$) and the lower limit value ($V_{Ik,min}$) of each input voltage level, respectively. That is, it is required to vary the V_{Ik} between $V_{Ik,max}$ and $V_{Ik,min}$ (voltage noise injection for voltage noise tolerance testing).

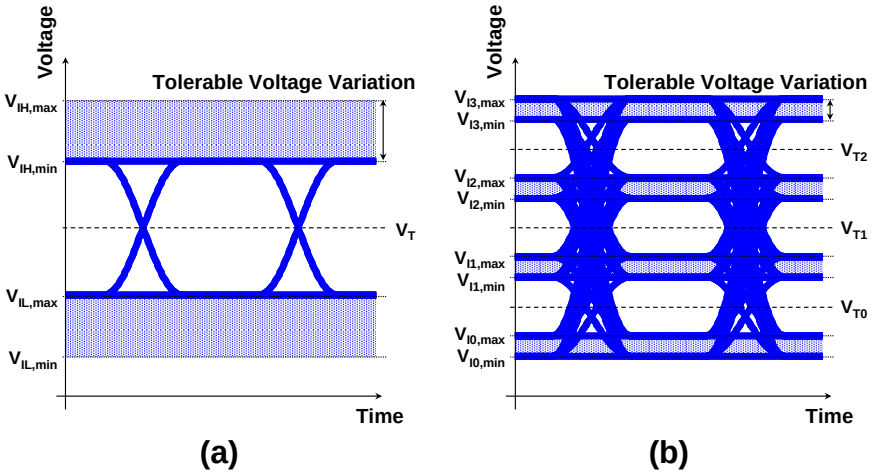

Figure 1: Voltage noise tolerance testing of the Rx Device. (a) Binary Signal. (b) Multi-level Signal.

Jitter Tolerance Testing: This tests the tolerance for the time variation of the input signals to an Rx device. For the jitter tolerance testing of the *multi-level* Rx devices, an already-proposed method [7] can be utilized.

In conventional jitter tolerance testing of binary signals, a jitter injection fluctuates the transient edge times T_{EDGE} of the input signal dynamically within a predetermined range (tolerable jitter) as shown in Figure 2(a). For the multi-level signal, multi-level voltage drivers that can inject jitter are required in the same way as for the binary signal. The data transient time of the multi-level signal is the boundary of data just as it is with a binary signal (Figure 2(b)). Therefore, for

injection of jitter to the multi-level signals, we may fluctuate the data transient time T_{EDGE} of the multi-level signal in the same way as for a binary signal. Hence, the same jitter injection method [7] as in a binary system can be applied to a multi-level signal.

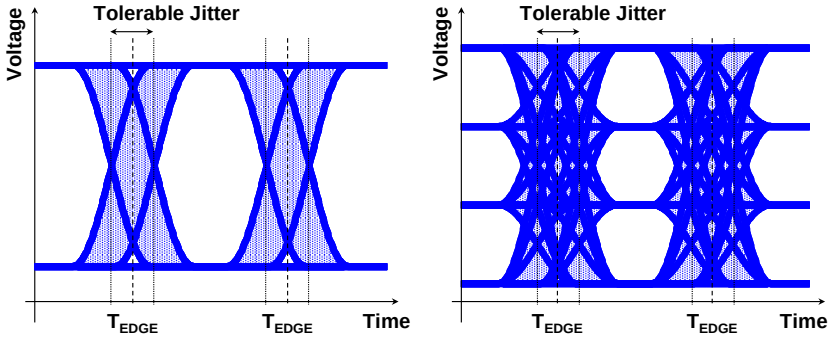

Figure 2: Jitter Tolerance Testing of the Rx Device. (a) Binary Signal. (b) Multi-level Signal.

2.2 Limitations of Conventional Test System

Figure 3 shows a conventional test system. The conventional system includes a pattern generator (PG), a timing generator (TG), a format controller (FC), voltage drivers (Dr), comparators (Cp), and a digital compare (DC). The PG generates test patterns input to the DUT and expected patterns for the output signal from the DUT. The TG generates high-precision times T_{EDGE} and T_{STRB}. The voltage drivers output binary test signals with two independent voltage levels (V_{IL} and V_{IH}) according to the waveform format generated by the FC based on the test patterns and T_{EDGE}. Two independent static threshold voltages (V_{OL} and V_{OH}) are supplied to two voltage comparators, respectively. The comparators compare the signal under test with the threshold voltages and sample the comparison logic at the strobe time T_{STRB}. A pair of comparators judges the voltage level of the signal under test as to where the level lies within the three areas delimited at the two threshold voltage levels. The sampled logic is compared with their expected pattern in the DC.

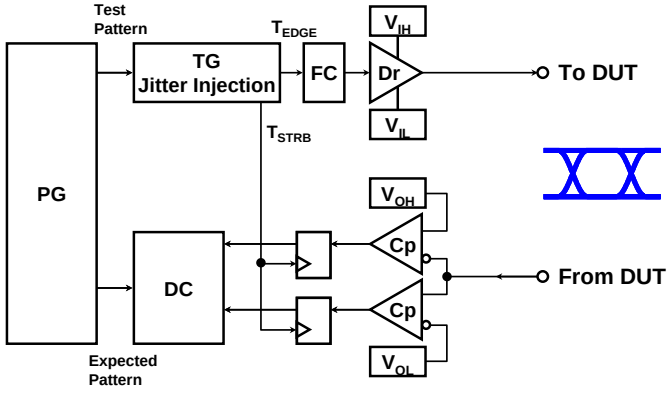

Figure 3: Conventional Test System for Binary Signals.

In order to generate the multi-level signals by using binary drivers, there is an existing method for generating an N-level signal, which combines $\log_2(N)$ driver outputs. Each driver output is weighted by a 2^n factor and then all are added together. For example, Figure 4 shows a 4-level signal driver with two binary driver resources. However, this conventional method utilizes a plural binary driver to generate a multi-level signal and therefore wastes driver resources. Since this method requires additional parts for the signal addition such as power combiners and timing resources for compensating time errors (skews) between signals to be added, test cost increase becomes a problem. Moreover, in the case of Figure 4, the fourth voltage level is determined by $v_1 + v_2$, which is the addition of v_1 and v_2, and therefore this method cannot set all voltage levels independently and cannot test multi-level signals flexibly. In order to set all voltage levels independently, a method for adding driver outputs in the thermometer code manner exists. However, it requires still more drivers. Thus,

these methods require more driver and timing resources, as the number of output voltage levels increases for voltage noise tolerance testing. Hence, the quality of the output signal degrades. Therefore, these methods are not suitable for a low-cost, high-accuracy solution.

Furthermore, output voltage levels of the driver in a conventional test system are fixed and cannot be changed dynamically (during the test execution) for voltage noise injection.

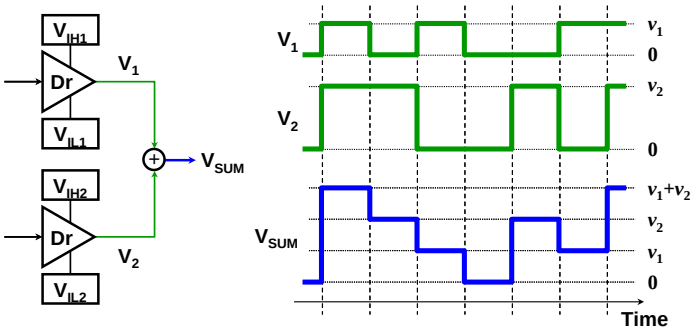

Figure 4: Generation of Multi-level Signals with Binary Drivers.

3. Proposed Test System

Figure 5 shows a proposed test system for a multi-level signal [8]. This test system includes multi-level drivers and multi-level comparators based on a dynamic threshold concept. The multi-level drivers can generate the multi-level signal and control its voltage levels and signal generation times flexibly. And, the multi-level comparators can also control threshold voltage levels and strobe times flexibly. The pattern generator of the system provides a plural bit of test patterns and expected patterns that represent a multi-level logic to a multi-level driver and comparator, respectively. A timing generator of the binary test system can be reused in this system.

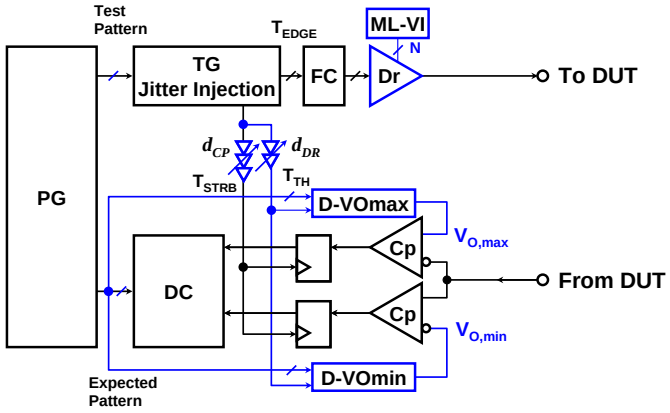

Figure 5: Proposed Test System for the Multi-level Signal.

3.1 Multi-level Driver

The proposed multi-level driver can set plural voltage levels independently for testing the functionality of multi-level signals. The output voltage levels are set by using the multi-level voltage input (ML-VI). This driver can also modulate each voltage level to inject voltage noise for testing the voltage noise tolerance of the Rx devices (Figure 6). Voltage level modulation is fast enough to test the tolerance of the Rx DUT for high-frequency deviation of voltage level.

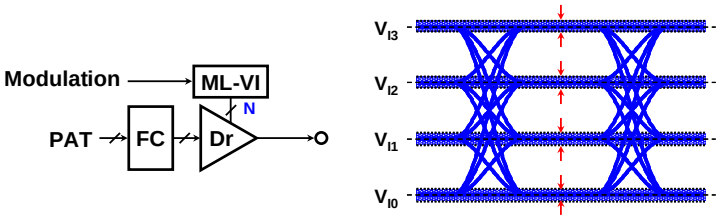

Figure 6: Voltage Noise Injection with Proposed Multi-level Signal Driver.

Since the proposed method can modulate each voltage level flexibly, it can inject the voltage noise with an arbitrary distribution. In addition, in the case of a differential voltage driver, by modulating the positive signal and the negative signal of the differential output signal independently, various types of noise can be injected. For example, while a random noise can be injected by modulating the positive and the negative signals independently each other, a common-mode noise can be injected by modulating them in the same phase (Figure 7(a)), and a normal-mode noise can be injected by modulating in the opposite phase (Figure 7(b)).

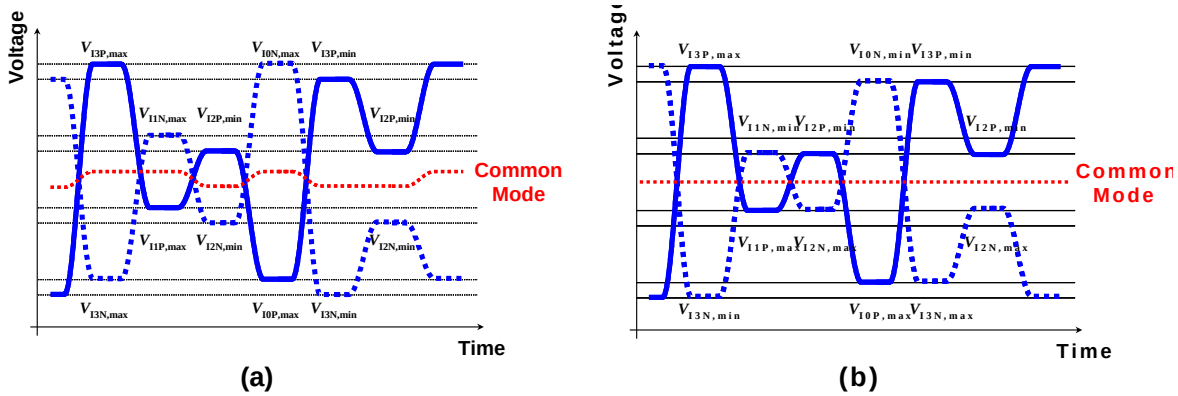

Figure 7: Noise Injection into Differential Signal. (a) Common-mode Noise. (b) Normal-mode Noise.

3.2 Timing Generator for Injecting Jitter

In order to test jitter tolerance of the receiver device, the multi-level driver can also modulate its output signal timings. The timing edge T_{EDGE} of the output signal is fluctuated by the jitter injection circuit built in the TG. Figure 8 shows a block diagram of the timing generator with jitter injection [7]. The TG is mainly composed of a digital integrator, a delay control logic and a variable vernier delay. Timing data extracted from a test pattern are accumulated by the digital integrator to determine a delay amount for each test cycle. The delay amount is divided into two components by dividing it by the reference clock period. The delay control logic delays the timing digitally according to the quotient part, and the vernier delay performs a fine timing adjustment by using the remainder part. Since the variable vernier delay is designed to accept different delay data at each test cycle, the edge timing for each test cycle can be changed cycle by cycle. Furthermore, since the timing information is digitally calculated, by adding jitter data into the original delay data, the edge timing is fluctuated cycle by cycle, and hence jitter injection is achieved.

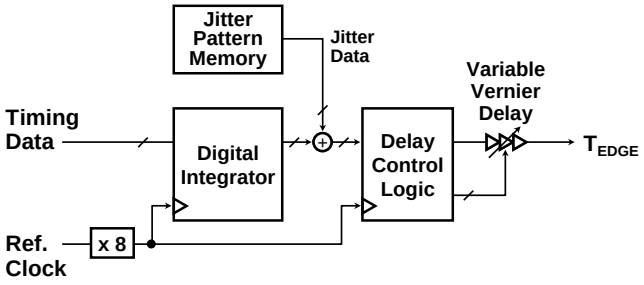

Figure 8: Block Diagram of Timing Generator with Jitter Injection.

4. Experiments

In this section, the experimental results with prototype circuit based on our proposed method are shown, and they demonstrate a concept of proposed test system for the multi-level signal.

4.1 Prototype Circuit

In order to demonstrate the proposed multi-level signal testing method, we fabricated a prototype circuit, including a 4-PAM driver and a 4-PAM comparator in 65nm standard CMOS process.

For the 4-PAM driver, a current mode logic (CML) driver was developed (Figure 9), in order to test the latest high-speed multi-level transceiver devices. Our CML driver has four inputs, one for offset control and three for amplitude control. The 4-PAM driver receives low-frequency test patterns, which are 2-bits wide in parallel, multiplexes them, and encodes then into thermometer codes to generate a 4-level PAM signal. By driving with the thermometer coding, our driver can eliminate the notch on the output waveform due to the switching skew between pattern control codes. On the other hand, voltage level modulation for the RX voltage noise tolerance testing is realized by modulating the digital control inputs of the current D/A converter (DAC) in the CML driver. For high-frequency modulation, some current DACs are used to inject voltage variation with dedicated modulation patterns.

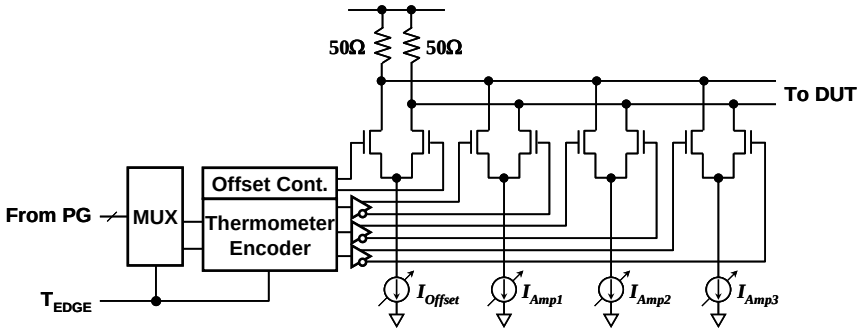

Figure 9: Prototype Multi-level Driver Circuit.

4.2 Experimental Setup

Figure 10 shows an experimental setup. A signal generator (ROHDE&SCHWARZ SMA100A, 6 GHz) provides 1 GHz Clock to the prototype circuit as its operating reference clock. The output signal of the multi-level driver is measured by a sampling oscilloscope (Tektronix CSA8000 with 80E04 sampling module). The maximum operating rate of the prototype circuit is 8 giga-symbols per second (16 Gbps at 4-PAM).

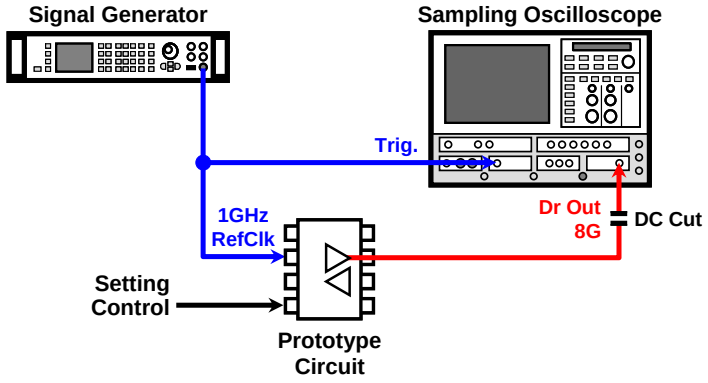

Figure 10: Experimental Setup.

4.3 Evaluation Results

4.3.1 4-PAM Signal Generation

The pseudo-random pattern of four voltage levels generated by the test pattern generator built into the prototype circuit is output, and the eye diagram of that signal was measured by using a sampling oscilloscope.

Figure 11 shows the result of the measurement of the eye diagram. The eye of 4-PAM signal was clearly opened. The variation of each voltage level of 4-PAM signal was 41.73 mV or less, and the jitter of the signal was 74.0 ps or less, at a 10^{-12} BER threshold. The eye opening in the voltage and time axis was 52.9 percent and 40.8 percent, respectively. The prototype driver has enough eye opening for the functional testing of Rx devices. Improving the settling characteristic of the driver can reduce the voltage variation and jitter still more. This is a future challenge of our development. As shown in Figure 12, each signal level can be set independently, and the intervals between each signal level can be flexibly changed.

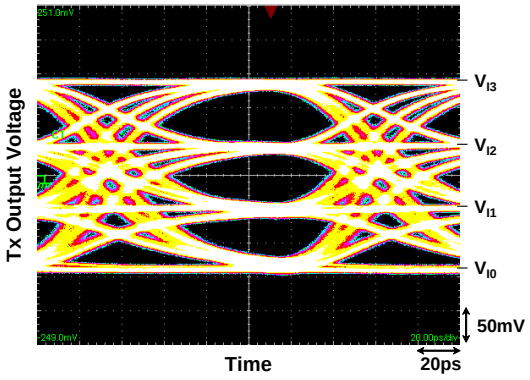

Figure 11: Eye Diagram of the Multi-level Driver Output Signal.

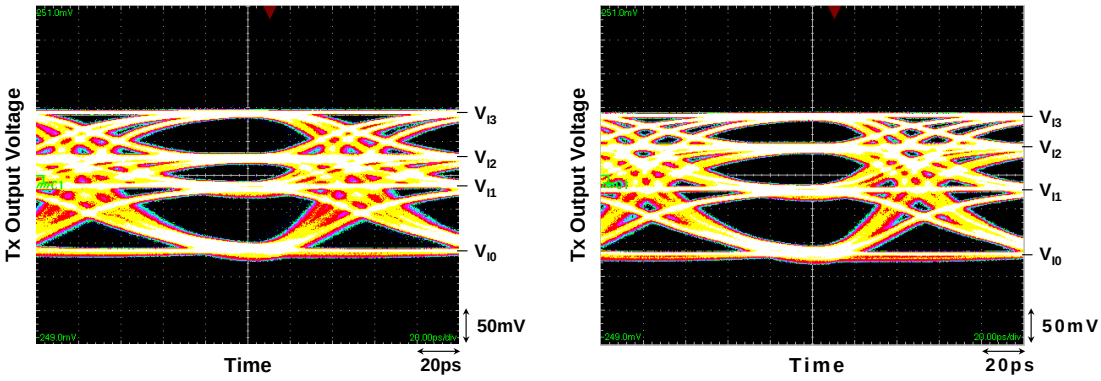

Figure 12: Generation of Multi-level Signals with Inequitable Interval between Voltage Levels.

4.3.2 Voltage Noise Tolerance Test Signal Generation

Next, the experiment of the proof of the concept of the voltage noise tolerance test signal generation was performed. A pseudo-random pattern of four voltage levels is generated, each voltage level of the generated signal was modulated to inject voltage noise.

Figure 13 shows the eye diagram of the voltage noise tolerance test signal. Figure 13(b) shows the eye in the case where each voltage level switches by two states (the upper limit value and the lower limit value.) It shows that the histogram of the voltage levels forms a double-delta distribution and therefore demonstrates the binary modulation. Figure 13(c) shows the eye in the case where each voltage level changes continuously between the upper limit value and the lower limit value. When the voltage level is modulated uniformly, the histogram of the voltage levels shows a uniform distribution. Signals with the voltage variation in a specified voltage range for four voltage levels have been generated. We have shown that the voltage noise tolerance test signal of multi-level Rx device can be generated by the prototype system.

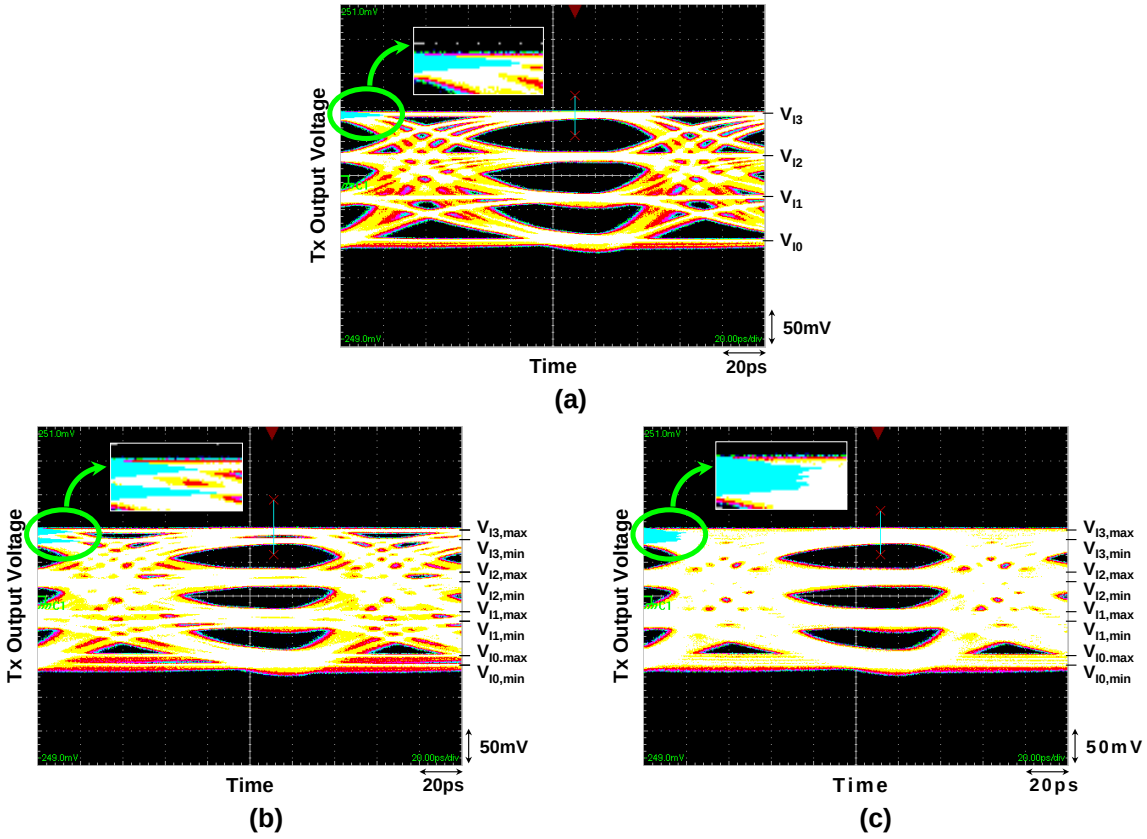

Figure 13: Eye Diagram of the Voltage Noise Tolerance Test Signal.
(a) No Modulation. (b) Binary Modulation. (c) Continuous Modulation.

4.3.3 Jitter Tolerance Test Signal Generation

Finally, the experiment for the jitter tolerance test signal generation was performed. A pseudo-random pattern of four voltage levels is generated, and the edge timing of the generated signal was modulated to inject jitter.

Figure 14 shows the eye diagrams of a clear 4-PAM signal and the corresponding jitter tolerance test signal. It shows that the jitter injected to the multi-level signal closes the signal eyes. An injected sinusoidal jitter with amplitude of 15.9 ps_{pp} closes the eye from 63.0 ps_{pp} to 41.5 ps_{pp}. The jitter amplitude error of 5.6ps_{pp} may be caused by an additional random timing noise component. We have shown that the jitter tolerance test signal for the multi-level receiver device can be generated by using the proposed test system.

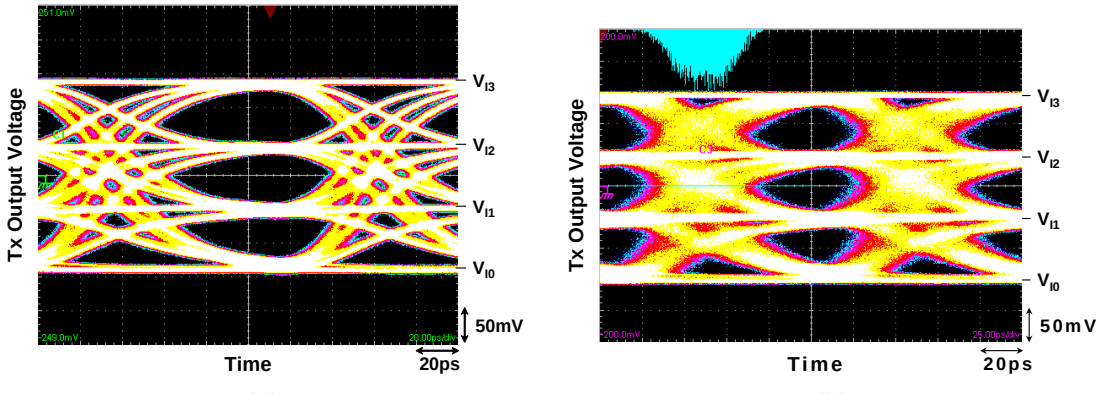

Figure 14: Eye Diagram of the Multi-level Driver Output Signal.
(a) Clear 4-PAM Signal. (b) Jitter Tolerance Test Signal.

5. Conclusion

In this article, a method for testing devices with multi-level signal interfaces was proposed. The proposed system has drivers that generate multi-level signals. The multi-level driver can perform the voltage noise tolerance testing and the jitter tolerance testing of the Rx devices with the multi-level signal interface. Experimental results with the prototype circuits show that the proposed system can achieve a real-time functional testing for the 16 Gbps 4-PAM signal and therefore shows the feasibility of the approach. This system is applicable to real-time testing of both binary signals and multi-level signals and is scalable to increase the number of voltage levels. Reducing noise and jitter of the multi-level driver is a future challenge for this development.

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