



Advantest IR Technical Briefing

# Future SoC Semiconductor Test Needs & Solutions

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# NOTE

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# Agenda

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- ✓ SoC Test: A Business in Transition
- ✓ The SoC Semiconductor Market Environment
- ✓ Future Test Needs & Solutions
- ✓ Summary



```
...mirror_mod.mirror_object = ...
operation == "MIRROR_X":
mirror_mod.use_x = True
mirror_mod.use_y = False
mirror_mod.use_z = False
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operation == "MIRROR_Z":
mirror_mod.use_x = False
mirror_mod.use_y = False
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print("please select exact...

OPERATOR CLASSES
```

# SoC Test: A Business in Transition

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# Operating Segment and Main Products / Solutions

## Semiconductor & Component Test System

### SoC Testers

**V93000**  
SoC Devices

**T2000**  
SoC Devices

**T6391**  
LCD/OLED Driver ICs



SoC: System on Chip. Used here to mean "non-memory devices."

### Memory Testers

**T5833**  
DRAM and NAND

**T5503HS2**  
High-Speed DRAM Test



## Mechatronics Systems

### Test Handlers

**M4872**  
High-End SoC /  
Automotive ICs

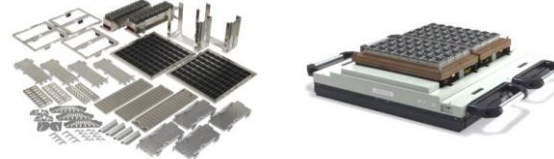
**M6242**  
Memory ICs



### Device Interfaces

Change Kit

HIFIX



### Nanotechnology

**E3650**  
CD-SEM for Photomasks / EUV Masks



## Services, Support & Others

### Maintenance / Service



**EM360**  
Service solution

### System Level Test

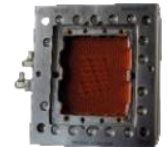
**MPT3000HVM**  
SSD System Level tester

**ATS503x**  
High-end SoC System  
Level tester



Thermal control unit

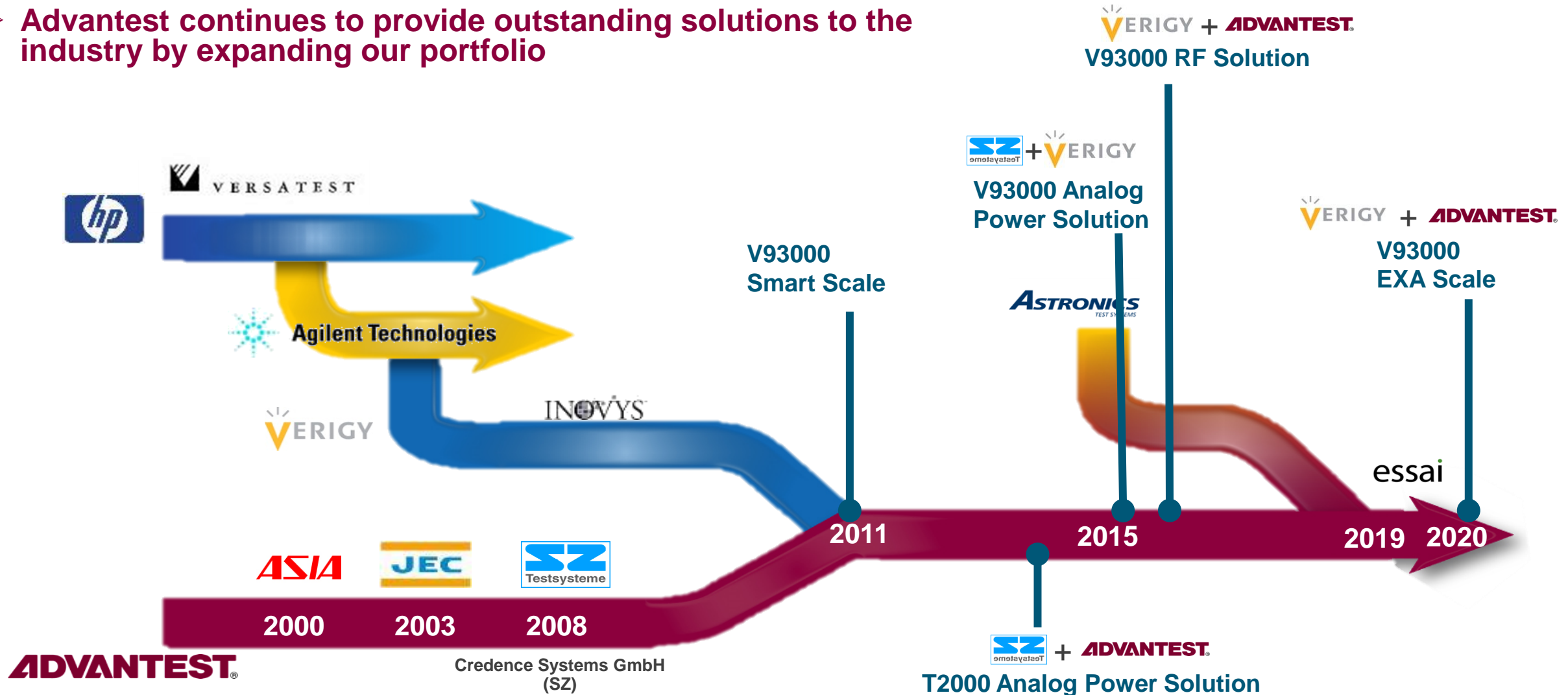
High-end SoC socket



Leasing / Second Hands Resale  
Other new initiatives

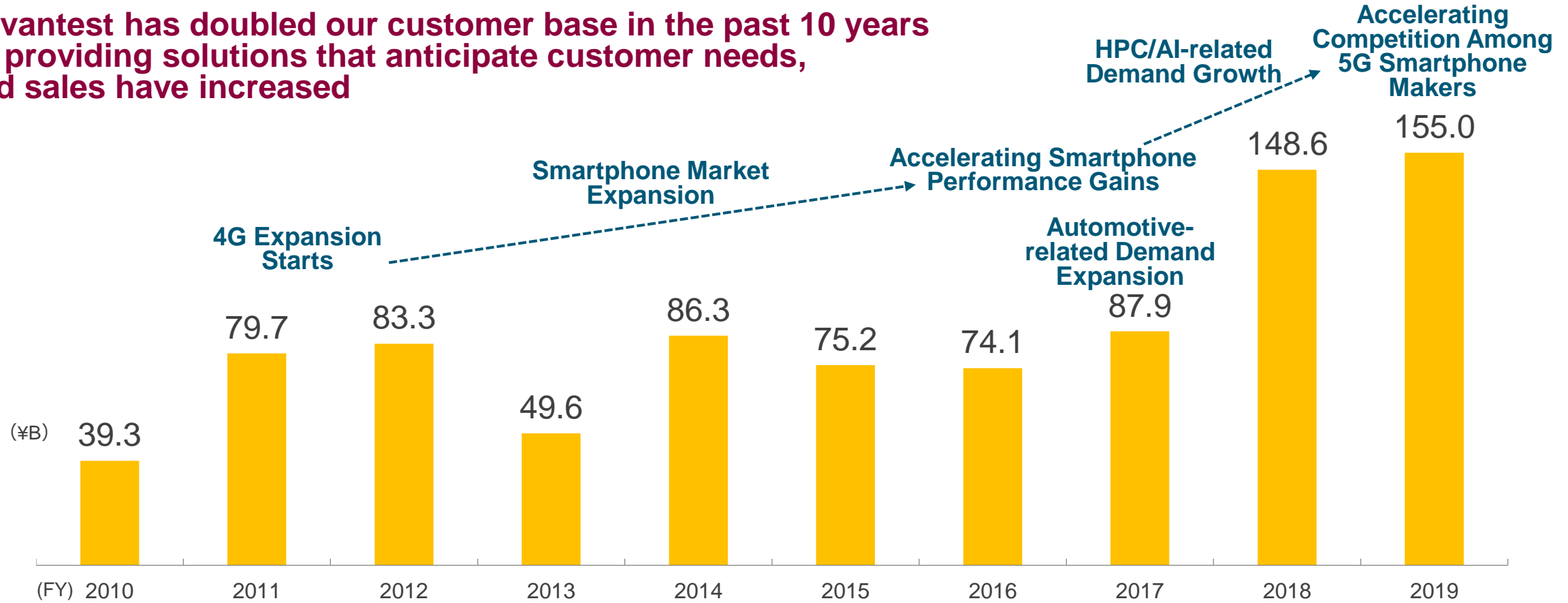
# R&D Synergy from M&A in Advantest's SoC Test Business

- Advantest continues to provide outstanding solutions to the industry by expanding our portfolio



# SoC Tester Sales Trends since 2010

➤ **Advantest has doubled our customer base in the past 10 years by providing solutions that anticipate customer needs, and sales have increased**



**Expanded customer base**  
with sales resources enhanced by M&A

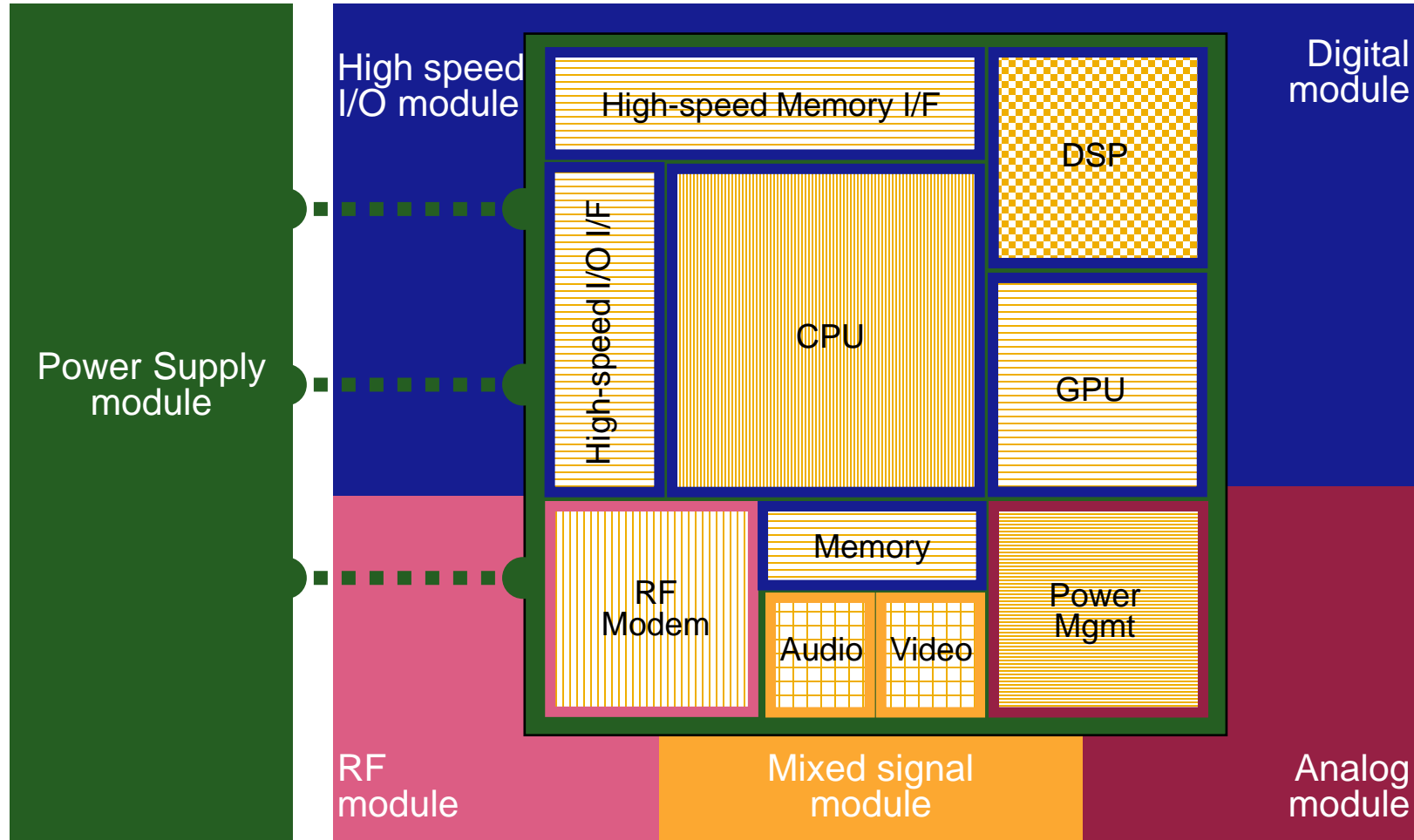
**Expanded solutions**  
with R&D resources enhanced by M&A

Expanded sales by capturing **more complex test requirements**  
from our growing customer base

**Acquired analog and power customers and accelerated design wins** with new solutions

**Launched high-performance DDIC\* products & dominated subsequent demand**

# SoC Testers That Support Test of Diverse IP



Basically, SoC semiconductor test checks that each function is operating correctly while passing a clean electric current through devices

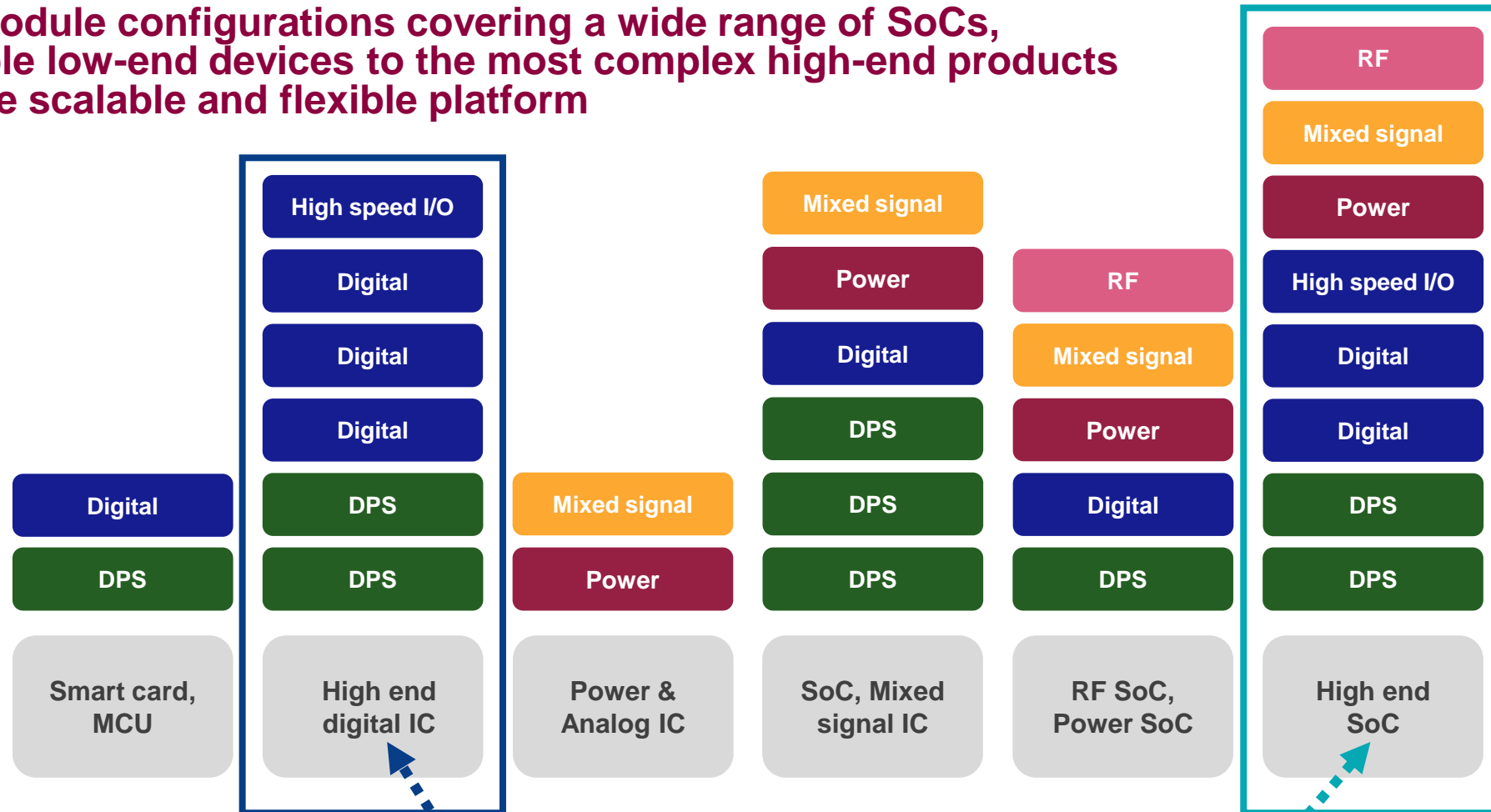
Test is performed by connecting a specialized module for each part of the SoC device: logic, analog, RF, etc.

Higher integration →  
greater test complexity



# Adding Value to SoC Test: Module Architecture

- Various module configurations covering a wide range of SoCs, from simple low-end devices to the most complex high-end products on a single scalable and flexible platform



More gates (cores) used in high-end logic ICs means longer test times

Advancing performance and complexity of large size SoCs (e.g. AI functionality) increases test times

# Advantest's SoC Tester Application Coverage

## Computing & Communications

Application processors (AP)

High-performance logic ICs (MPU/GPU/AI/FPGA)

RF devices (WiFi, Bluetooth, mmWave...)

## Automotive / Industrial / Consumer

Standard logic ICs (MCU, Smart Card...)

CMOS image sensors (CIS)

Display driver ICs (DDIC)

Analog / mixed signal ICs

Power management ICs (PMIC)

Module functions are optimized for each application  
A wide range of applications can be measured by switching out modules



V93000



T2000

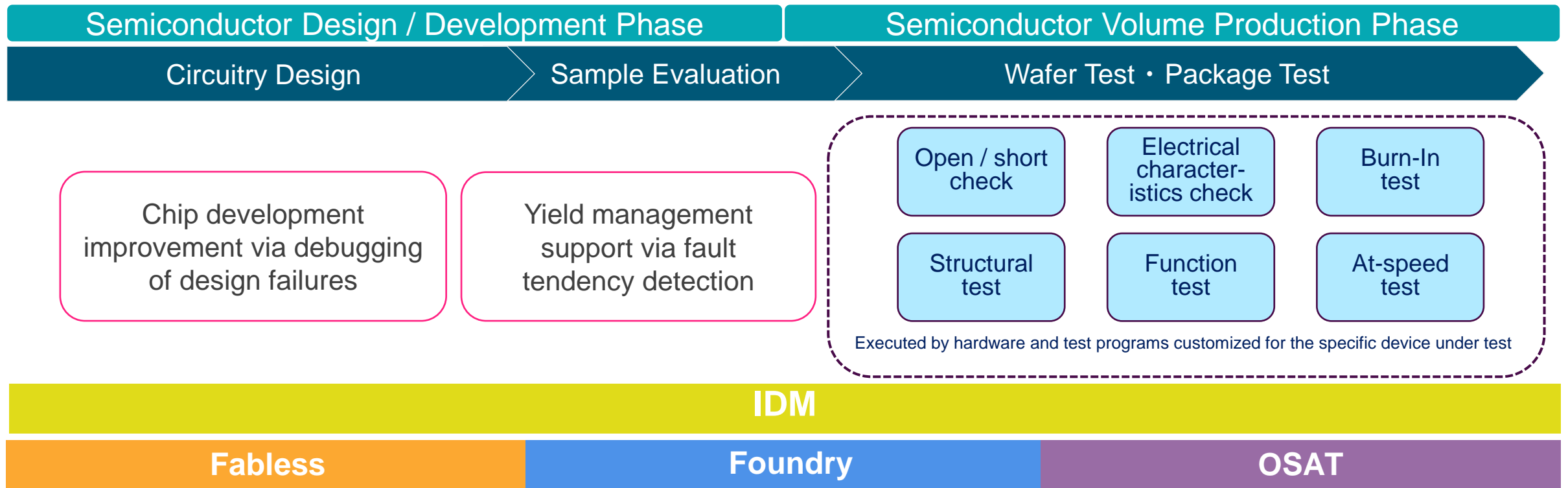


T6391  
(dedicated DDIC tester)



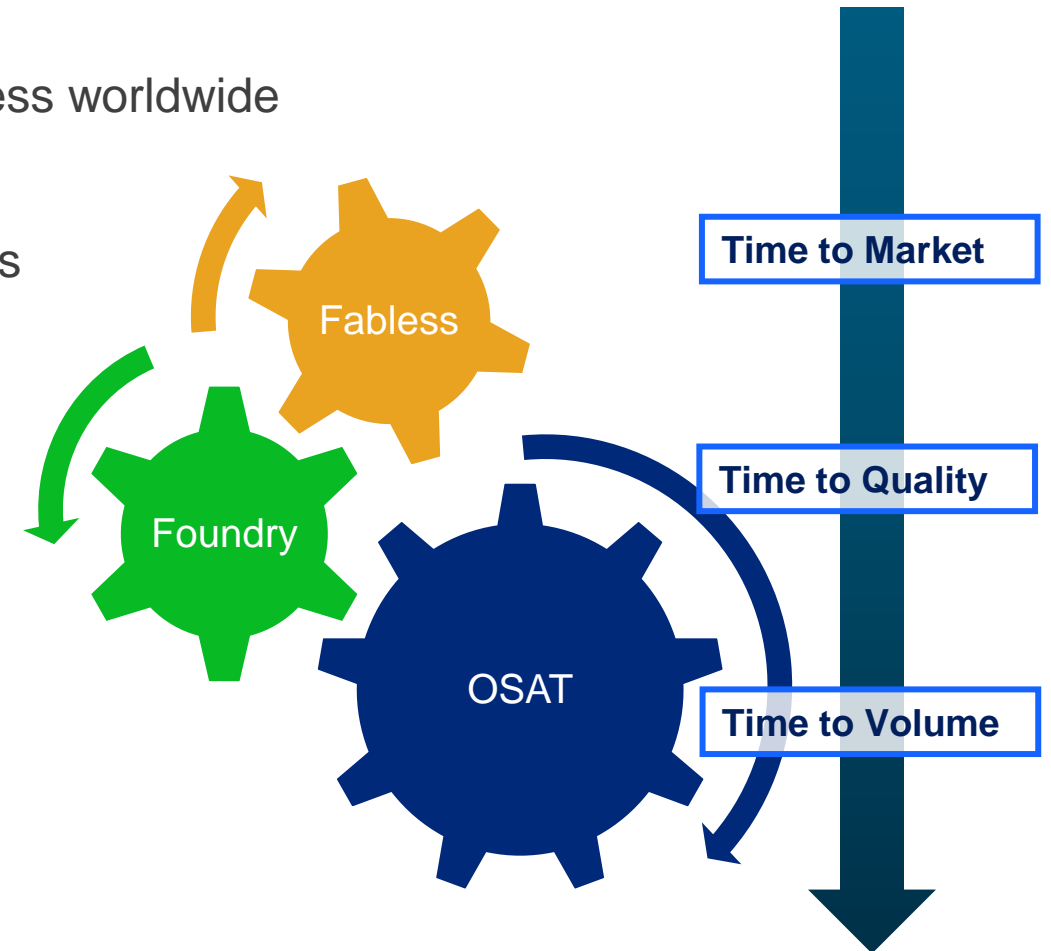
# Where Testers are Used: From Customer Lab to Fab

- Testing is essential for all semiconductors
- Through highly precise electronic signal analysis, Advantest's semiconductor test systems contribute to product quality improvement and control, performance measurement and improvement, time-to-market reduction, and production yield increases, throughout customer workflows from R&D to volume production



# Engineering Consultations Support Semiconductor Market Growth

- ✓ More than 600 test engineers support our customers' business worldwide
- ✓ As the evolution of semiconductors increases the difficulty of test, we provide consultations on appropriate test methods and environments for the latest semiconductors.
  - Seamless technical support from design / evaluation to volume production fabs
  - Integrated solutions that include peripherals, leading the industry in measurement reliability and efficiency
- ✓ Test trend data is fed back to the R&D teams developing next-generation testers to benefit customers



**Close partnerships with a broad range of customers drive mutual growth**

# Advantest's Core Competences Support SoC Evolution

## ➤ Industry's No.1 technological capabilities & leadership

- ✓ SoC semiconductor test equipment market share > 50% (2018-2019) (Advantest estimate)
- ✓ Dominant position in the high-end market where test technology requirements are most demanding
- ✓ Industry-leading MTBF (Mean Time Between Failure)

## ➤ Industry's No.1 customer base and largest installed base

- ✓ Advantest has built up a strong customer base including IDMs, fables, foundries, and OSATs
- ✓ Number of volume production systems in operation worldwide is industry's greatest

## ➤ Total solutions including test peripherals and a global support network

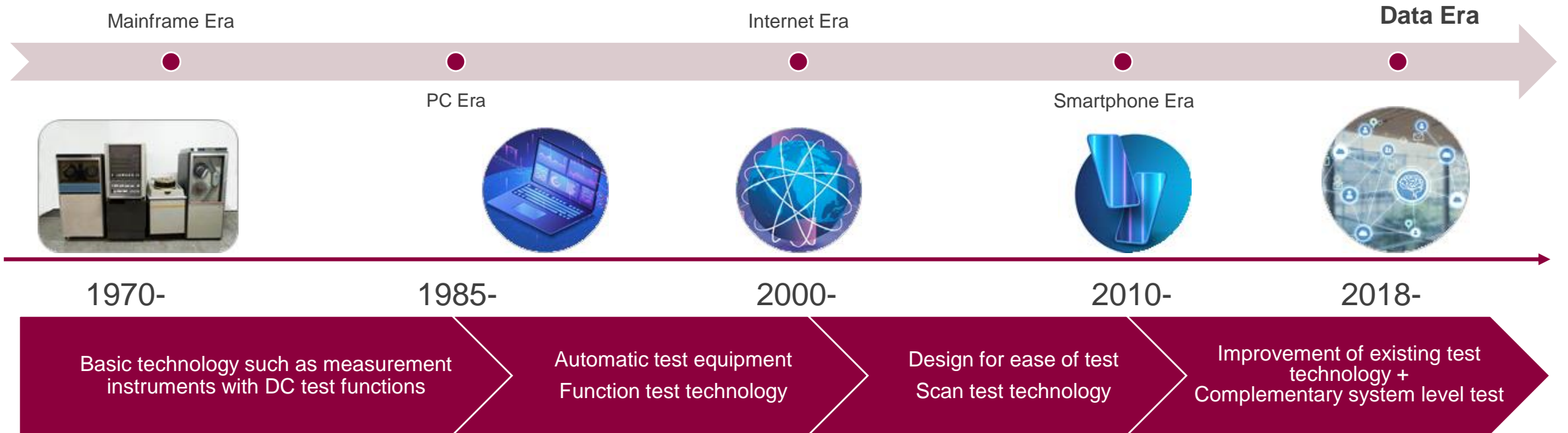
- ✓ Ranked No. 1 in VLSIresearch customer satisfaction survey, and ranked in "Best 10" for 32 consecutive years
- ✓ One-stop global support for test systems, test handlers, and device interfaces operating as a comprehensive test environment



2018 Global Technology Leader  
Thomson Reuters Top 100



# Evolving Electronics, Evolving Test Technology



- ✓ In the 2020s, not only 5G but also AI will be widely adopted, and data center / data server processing capacity will improve
- ✓ Technology leaders will accelerate innovation
- ✓ Synergy from diverse IP and advanced package adoption are two trends requiring more powerful test capabilities and measurement environments

**Advantest aims to predict transitions from one technology era to the next (“Waves”) and add customer value in an evolving semiconductor value chain**

The background features a network diagram on the left with nodes and connecting lines. Overlaid on this are several lines of code in a light gray font, including: `mirror_mod.mirror_object = ...`, `operation == "MIRROR_X":`, `mirror_mod.use_x = True`, `mirror_mod.use_y = False`, `mirror_mod.use_z = False`, `operation == "MIRROR_Y":`, `mirror_mod.use_x = False`, `mirror_mod.use_y = True`, `mirror_mod.use_z = False`, `operation == "MIRROR_Z":`, `mirror_mod.use_x = False`, `mirror_mod.use_y = False`, `mirror_mod.use_z = True`, `selection at the end -add ...`, `obj.select= 1`, `obj.select=1`, `context.scene.objects.active`, `obj.context.selected_objects`, `obj.name]`, and `print("please select exact")`.

# The SoC Semiconductor Market Environment

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# Semiconductors Support Changing Lifestyles



**Contributing to the safety, security, and comfort of the general public through measurement technology**



# Applications Driving the Next-Generation SoC Market



High performance and high functionality are required of SoCs in all arenas

# High-End Processors That Support Smart Lifestyles

## Smartphones

Computing performance that supports 5G



- Utilization of state-of-the-art process nodes
- Faster interfaces
- Balance of performance and power consumption

## Big Data Processing

Packaging that achieves high performance



- Adoption of state-of-the-art packaging techniques (Chiplets, 2.5D / 3D)
- High power and thermal control

Next-generation architecture that achieves ultra-high-speed processing



- Million-core architectures
- Parallel processing and scalability
- Power domain control

# Semiconductors Power Next-Gen Automotive Technologies

## Safety & Security Guaranteed

### The Zero Defects Principle

- ✓ Market failures: 0
- ✓ In-process failures: 0
- ✓ Accidents: 0



## Zero Emissions

### Electric cars (HV/PHV/BEV)

- ✓ Car weight reductions
- ✓ 12V batteries ⇒ 48V batteries
- ✓ Efficient motor drives

## Self-Drive is Coming

### ADAS/Autonomous Cars

- ✓ More high-sensitivity sensors
- ✓ Advanced CPUs
- ✓ Automotive package proposals
- ✓ Automotive networks speeding up

## Networkification

### The Connected Car

- ✓ Communications with the outside of the car
- ✓ GPS location information
- ✓ Big data processing in the cloud
- ✓ Networked with other applications

**It is necessary to expand the application range of semiconductors that support CASE\*, and further improve functionality, performance, and reliability**

# Further Expansion Expected in Image Sensor Market

- Market growth is expected as technological innovation continues, centered on smartphones
- Applications are expanding across various fields such as automotive, AR / VR, security, and drones

## Smartphone Market



Multiple cameras

By 2024, 80% of smartphones will be triple camera phones

Higher speeds

Transition from MIPI\* D-PHY to C-PHY

>100M pixels

4K/8K videos

### [The merits of using C-PHY]

- 1) Data rate about 1.5 times that of D-PHY
- 2) High-capacity data communications and high speed allow reduction of data line wiring area
- 3) Lower power consumption during transmission and reception
- 4) More flexibility in circuit layouts

\*MIPI=Mobile Industry Processor Interface Alliance

## Emerging market



Automotive

Core technology for autonomous car

Application Expansion

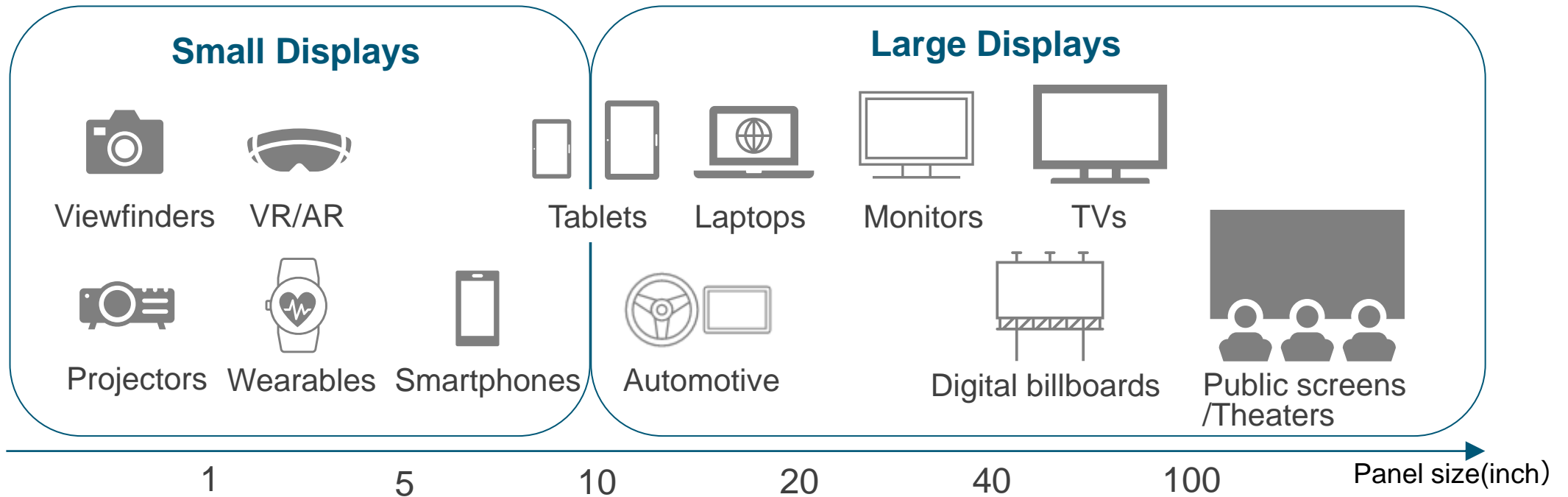
AR/VR, Security, industrial drones etc.

Intelligent Image sensor

Integration of Edge AI

# The Growing Display Market & DDIC Demand

- Drivers of display demand: The shift to 5G, the trend toward 4K / 8K TVs, the acceleration of DX due to greater WFH adoption



## Advanced technology driving the expansion of the display market

- ✓ High-resolution display technology that achieves WQHD, 4K / 8K
- ✓ High-speed data transfer technology for better image quality: MIPI C/D-PHY for smartphones and dedicated high-speed I/F for TV
- ✓ Integration of DDIC, touch sensors, and fingerprint sensors
- ✓ Bezel-less displays for TVs and smartphones



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..._ob.select = 0
... bpy.context.selected_...
...nt("please select obj...

...OPERATOR CLASSES...
```

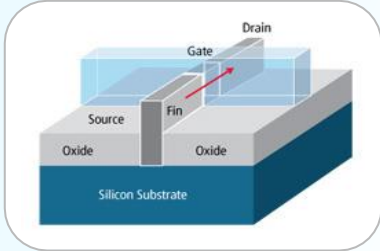
# Future Test Needs & Solutions

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# Test Challenges Resulting From SoC Product Evolution

## Quality Assurance Reinforcement

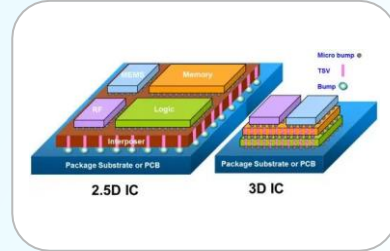
### Advanced Processes



**Enormous increases in transistor counts**

Huge numbers of test patterns are necessary to check the operation of all transistors

### Advanced Packages

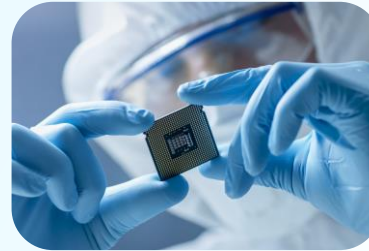


**2.5D/3D packaging**

High-precision test needed to detect failure modes specific to advanced packages

## Analysis Capability Reinforcement

### Advanced Production Line Ramps



**Yield improvements that meet TTM\* needs**

Huge amounts of test result data are needed to improve yields by refining manufacturing processes

\*Time To Market

## Performance Assurance Reinforcement

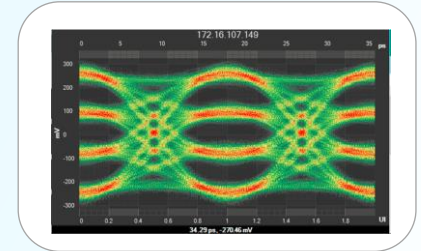
### High Reliability Needs



**Achieving zero defects**

Highly accurate test environments are needed to detect every failure

### Higher Performance & Functionality



**Dramatic improvements in operating speed, etc.**

Actual operation level test needs must be applied to guarantee the required performance

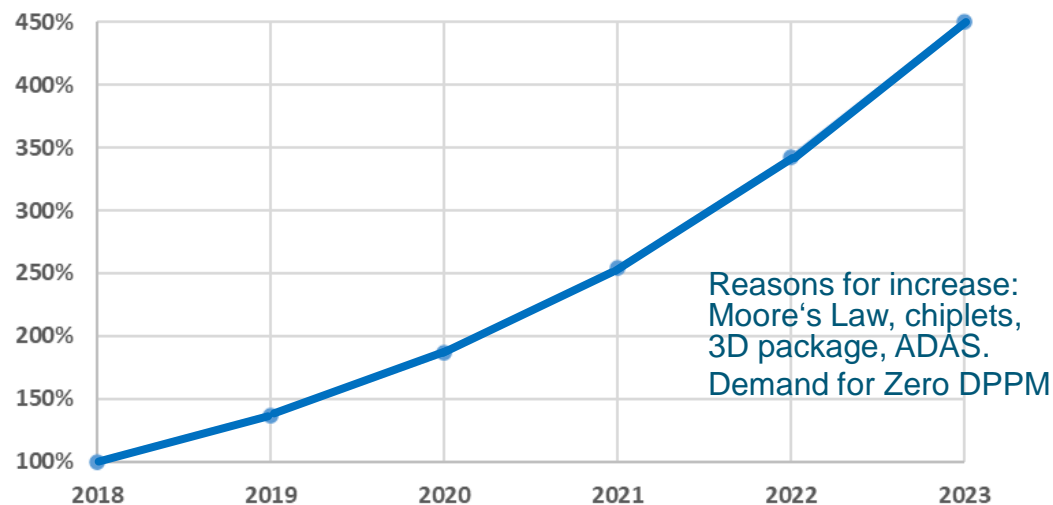
**As SoC products evolve, makers need to achieve higher quality and performance assurance using ATE**

# High-End SoC Device Test Challenges ①

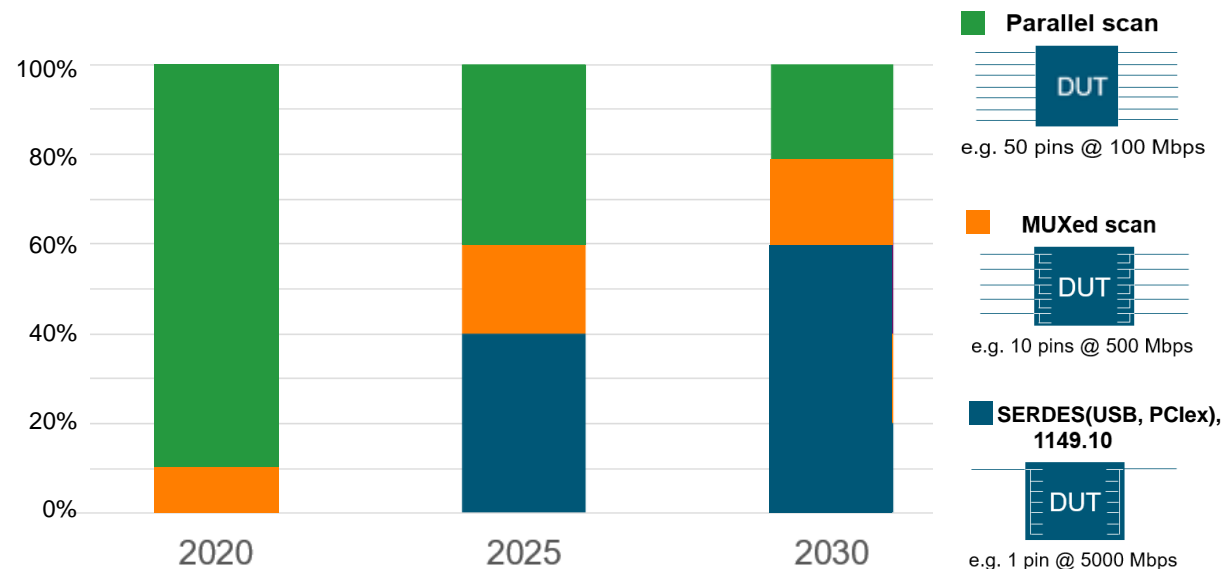
## ➤ New Scan Test Challenges

### Scan test pattern growth

Relative scan volume growth (SoC, max)



### Requirements for high-speed serial interfaces for scan test



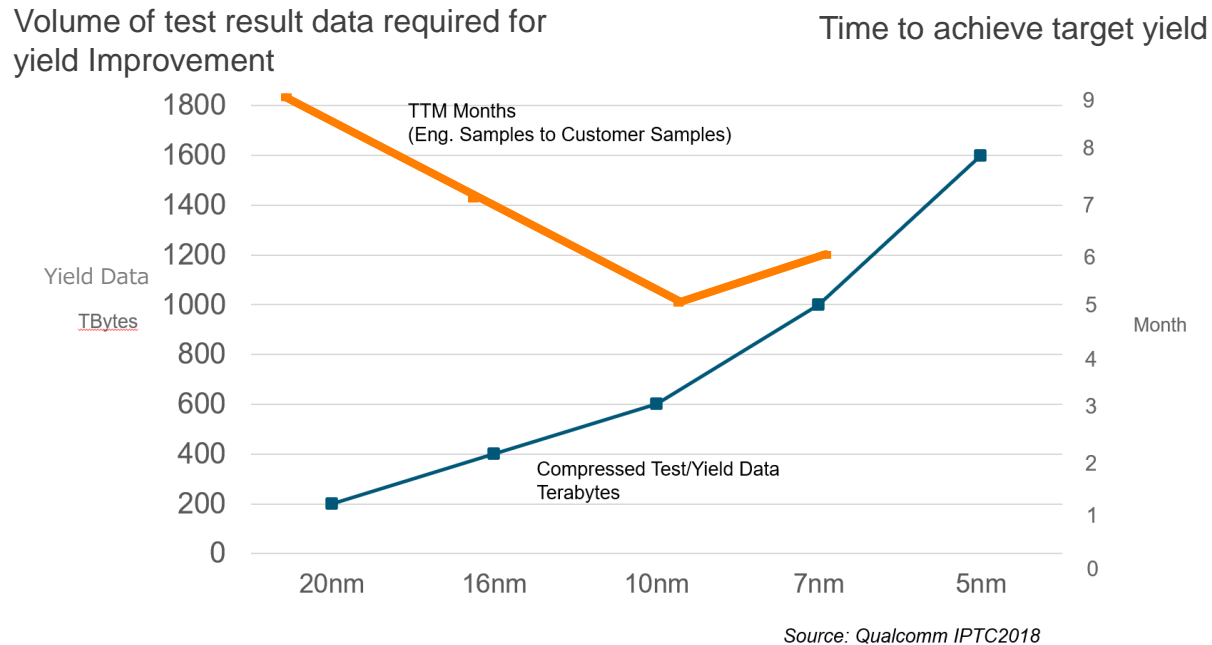
Scan test is the primary type of structured test applied to logic circuits. The scale of the logic circuits used in SoC devices is rapidly increasing, and so is the scale of test pattern, making it impossible to achieve a failure detection rate sufficient for quality assurance with manually created functional test data. Therefore, scan test has become a necessary prerequisite for SoC test.



# High-End SoC Device Test Challenges ②

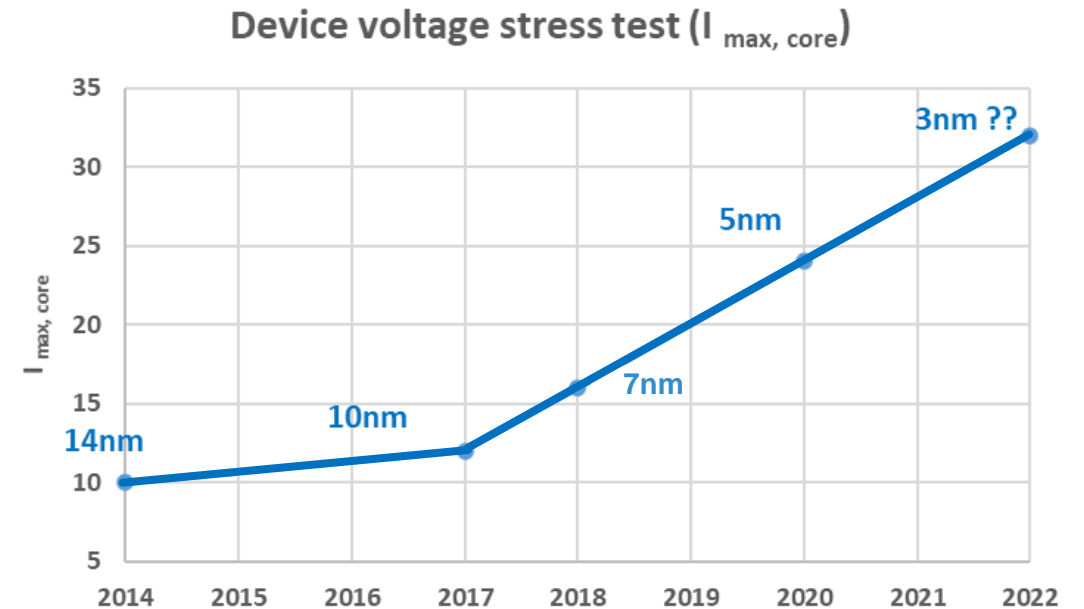
- Miniaturization of devices makes it important to acquire and analyze huge amounts of test data
- Higher integration also increases power consumption (>1000W: multiple types of power domains supported)

## Advanced process node development times (ES~CS)



Process shrinks have dramatically increased the volume of test result data required for yield improvement.

## Process shrinks require higher power



Electrical current consumption per power domain is increasing.

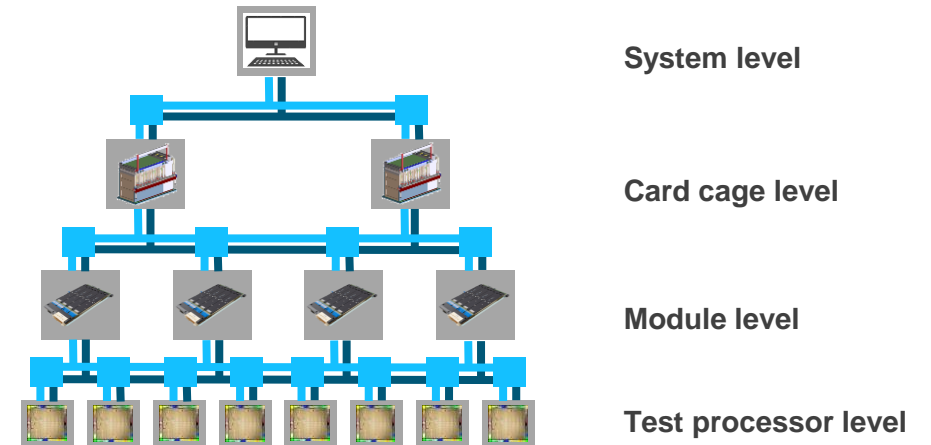
# Enabling Leading-Edge Technologies

## Advanced packages powering the newest modules deliver innovative performance evolution



- 16 completely independent pins are mounted in a small space, with 256 pins--twice the pin count of previous products--mounted in one module
- Utilizes high-speed core to support high-speed serial scan test up to 5Gbps
- Multi-core processors such as MIPS processor core and DSP core are also installed to speed up calculation processing, achieving greater multifunctionality and higher-performance test functionality.

## Adoption of a distributed computer network inside the tester improves the efficiency of parallel test



- Improve test throughput by means of decentralization of processing and communication, instead of only by the system controller
- Parallel setting and parallel processing increase the efficiency of multi-site test
- As the volume of test data such as scan increases, so does the volume of test result data. Data upload / download is now faster.

# Advantest Debuts the V93000 EXA Scale™

- **The new platform implements all the functions required to meet next-generation semiconductor test challenges**

## Deepest vector memory

- All pins have deep vector memory
- Integrated multi-pin memory enables even larger scan tests

## Industry-leading digital pins

- Scan test speed of 5Gbps
- High speed scan test & existing functional test capabilities

## Covers all power requirements with a single DPS card

- Broaden current supply capability(mA range to several KA)
- Excellent accuracy and responsiveness (instantly compensates for voltage fluctuations, improving yield)
- Innovative probe needle protection



## Throughput optimization

- Dual sequencer enables highly efficient operation
- High-speed failure data capture

## Outstanding scalability

- From small engineering configurations, to large configurations for volume production

## Broad application coverage

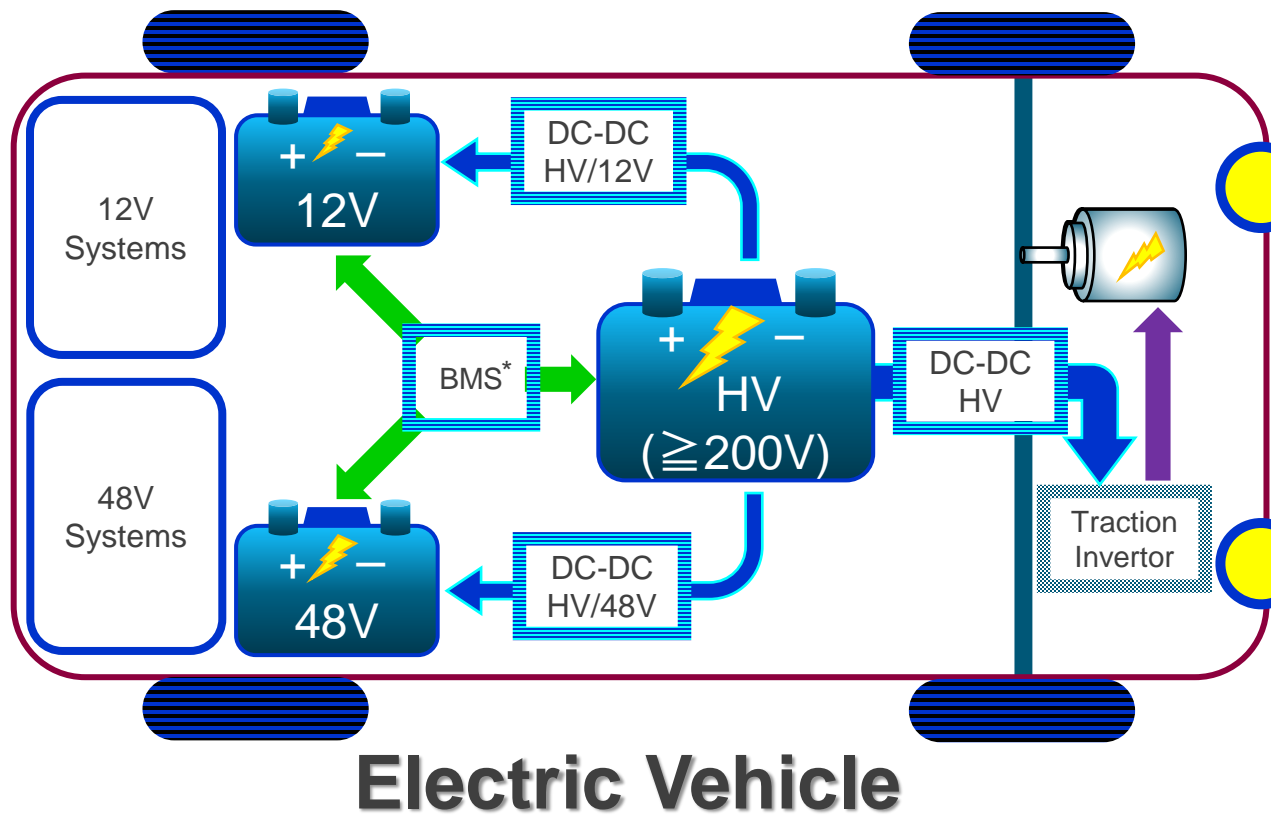
- Also supports high-speed test and RF test

## Compatible with existing V93000 DUT boards

DUT boards can be shared between EXA Scale and Smart Scale systems, eliminating migration barriers

# Technical Requirements for Automotive Electronics

- **The response to the shift to EVs and the introduction / evolution of autonomous driving technology**
  - Better mileage: Support for a wide range of voltages by further increasing the performance and capacity of Li-ion batteries
  - More automotive ICs / electronic components: High efficiency and energy-saving performance required for each device



**Electric Vehicle**

\*BMS: Battery Management system

## T2000 Automotive Test Solutions



T2000 AiR

### Test Module Family

- SHV2KV
- MFHPE
- MMXHE

## V93000 Automotive Solutions



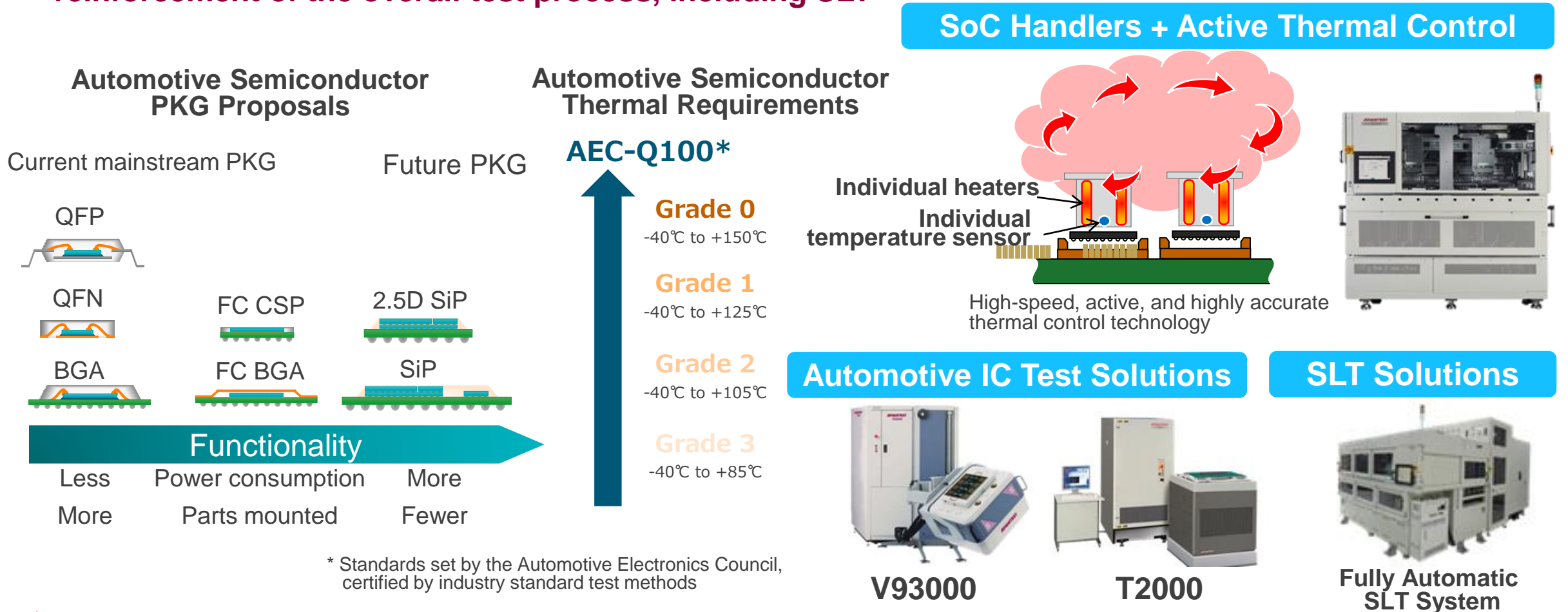
A-Class

### Test Module Family

- HV800
- FVI16
- AVI64

# New Automotive Semiconductor Test Challenges

- Advantest's handlers offer high precision, active thermal control and handling of various packages required by all automotive grades
- The miniaturization of ADAS processors and the adoption of advanced packaging methods require reinforcement of the overall test process, including SLT



# CIS Test Challenges & Advantest's Solutions

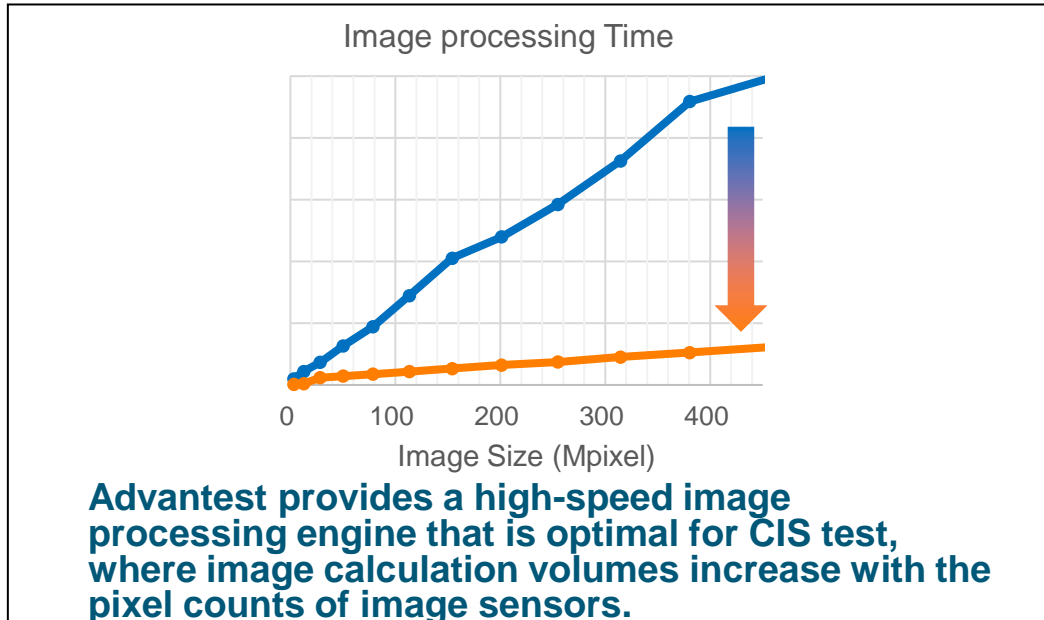
## Test challenges resulting from the further evolution of cameras

- ✓ Support for higher resolutions used in high-end smartphone cameras  
(Resolutions are expected to increase at a pace of 100 million pixels per year )
  - ➔ Need to suppress test time increases and reduce test cost
- ✓ Support for faster interfaces that handle increasing data transmission volumes
  - ➔ Now: D-PHY 4.5Gbps / C-PHY 3.5Gbps
  - ➔ Future: D-PHY 9.0Gbps / C-PHY 6.0Gbps



**T2000 ISS**

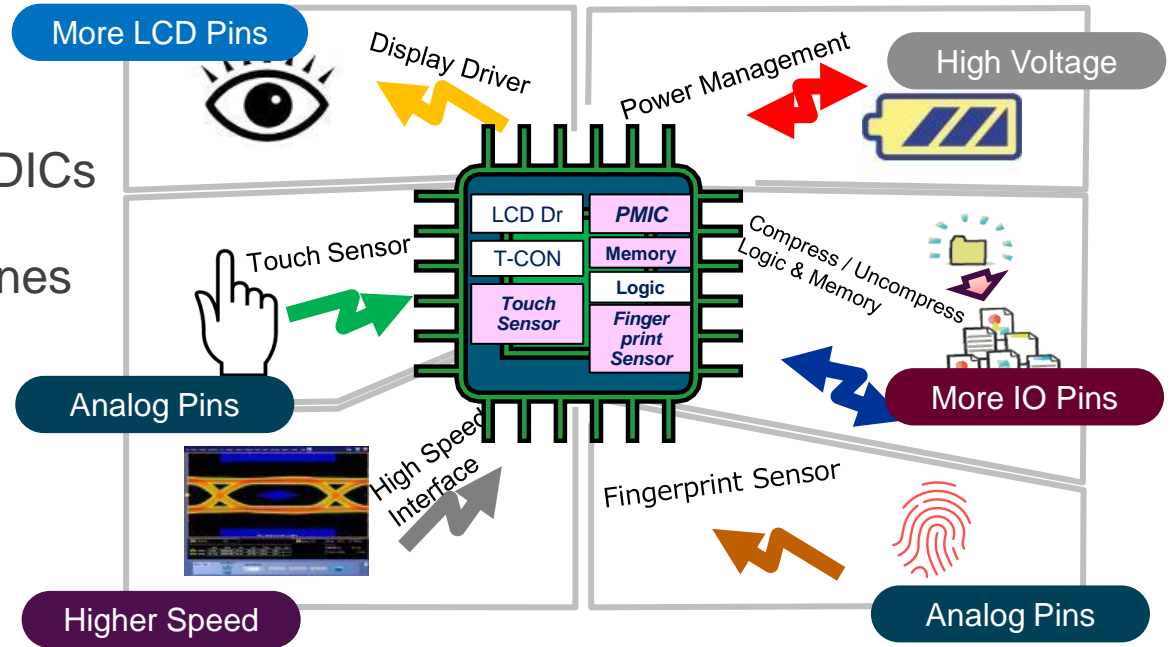
**CMOS Image Sensor Solution**



# DDIC Test Challenges & Advantest's Solutions

## Display Technology Evolution Creates New DDIC Test Challenges

- High-precision multi-pin measurement capability for DDICs for high-resolution displays
- High-speed I / F measurement capability for smartphones and TVs
- Analog characteristic measurement capability for DDICs with integrated touch sensors and fingerprint sensors



## All-In-One Solution for DDIC Test : the T6391

- Industry-leading 3,584 LCD pins achieved by applying multi-pin contact technology used in SoC testers
- Equipped with a high-speed I/F measurement option (6.5 Gbps) that supports test of all high-speed I/F standards for smartphone and TV displays
- Offers an analog measurement option for touch sensor and fingerprint sensor test



# Summary of Semiconductor & Tester Performance Innovations

Innovations in SoC Semiconductor Technology	Innovations in SoC Tester Performance
<p>General</p> <ul style="list-style-type: none"> <li>Increasing transistor counts due to miniaturization</li> <li>Larger-scale semiconductor circuits mean larger current supply and multiple IPs on one chip</li> <li>Faster interfaces</li> <li>Higher frequencies, data processing speed improvements (high-speed data transfer)</li> <li>Enhanced reliability (demand for mission-critical applications is growing)</li> </ul>	<ul style="list-style-type: none"> <li>Power supply module flexibility supports larger-scale semiconductor circuits</li> <li>Support for multiple domains for installation of multiple IPs</li> <li>Enhanced dynamic response and accuracy for new failure mode detection and yield improvement</li> <li>Enhanced lineup of measurement modules</li> <li>Reinforced high-speed interface test to address increasing data volumes and test data speed</li> <li>Industry-leading platform flexibility and scalability</li> </ul>
<p>High-End Processors</p> <ul style="list-style-type: none"> <li>Adoption of advanced processes, higher integration</li> <li>Adoption of advanced packaging (chiplets, memory I / F with higher speeds and lower power consumption)</li> </ul>	<ul style="list-style-type: none"> <li>Better high-speed test result capture with superior throughput addresses the increased importance of failure analysis and yield improvement stemming from the adoption of advanced processes</li> <li>Support for large data capacity, high-speed scan test</li> <li>Broaden current supply capability (mA range to several KA)</li> <li>Support for more demand for SLT test processes</li> </ul>
<p>Automotive Semiconductors</p> <ul style="list-style-type: none"> <li>Expanding semiconductor applications, automotive grade temperature control</li> <li>Autonomous driving</li> <li>BVE</li> <li>Connected car technology</li> <li>Diverse package development</li> </ul>	<ul style="list-style-type: none"> <li>Achieve high-end processor equivalent test coverage in the autonomous driving processor market</li> <li>In order to achieve zero DPPM, the quality required for vehicles, it is necessary to increase test times. Support for high precision ,active thermal control technology during test. Strengthening of overall test flows including SLT</li> <li>With the adoption of EVs, the measurement range for large currents and high voltages has grown</li> </ul>
<p>CMOS Image Sensors</p> <ul style="list-style-type: none"> <li>Adoption of C-PHY (new data interface)</li> <li>Higher pixel counts and higher resolution</li> <li>Expanding applications for sensing technology</li> </ul>	<ul style="list-style-type: none"> <li>Faster interfaces to handle larger data transfer volumes</li> <li>Better calculation processing throughput to keep up with increasing image data size</li> <li>Strengthening of logic functions for increasingly widespread AI-equipped CMOS image sensors</li> </ul>
<p>Display driver ICs</p> <ul style="list-style-type: none"> <li>High-speed data transfer technology that achieves high resolution and high image quality</li> <li>Multiple functions on a single chip</li> </ul>	<ul style="list-style-type: none"> <li>Support for all high-speed display interfaces</li> <li>Improved analog measurement functions</li> <li>Enhanced logic functions to support mounting of touch sensors, fingerprint sensors, etc. on chips</li> </ul>



# Big-Picture Summary

