Advantest Corporation
IR Technical Briefing
Q&A Summary

December 7, 2022

Q: I understand that your company has a leadership position in the High-performance computing (HPC) tester market. The SoC test market overall is dominated by Advantest and one other company. Could you elaborate regarding your technological advantages over your competitor which could result in future market share gains?

A: We believe that the superiority of the V93000 is due to two factors.

First, platform advantages. When the V93000 was first launched, the subcontract manufacturing model, which is a new business model where development and production were split across different companies, was taking off in the semiconductor industry. Our broad system scalability and performance across a very wide range on a single platform meets the diverse and wide-ranging test needs of the Outsourced Assembly & Test (OSAT) customers who took on a key role under this model, who are responsible for semiconductor packaging and test processes. In addition, we were the first in the industry to achieve long-term compatibility with a single test platform, which is crucial for customers when migrating to the next generation of testers. Being able to provide such solutions is a cornerstone of our leadership.

Meanwhile, in terms of technological superiority, there is a strong demand for testers that can test a wide range of computing devices, from chips for PCs and smartphones to servers and AI, as often as necessary per device, and support for device power supplies is also a key factor.

In our tester R&D, we have always emphasized open development over a long period of time. We have continually secured and maintained a lead over our competitors by improving the functionality of testers one step ahead and providing solutions for the highly functional semiconductors our customers develop. We believe that our leadership is also based on these technologies and testing methodologies.

In today's presentation, we discussed how to actually provide a link partner for computation to the device under test on the tester. These various methodologies for interaction with devices are completely new fields that have never existed before. We plan to explore new testing methodologies for dynamic architectures and solve problems such as how to connect devices efficiently.

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We participate in multiple industry consortiums and are closely watching what the leaders of these industries will do. Together with them and our customers, we are developing new test methodologies that go beyond traditional ATE (Automated Test Equipment). We anticipate that test methodologies will be improved and developed in various ways in the future, and we believe that Advantest will lead these changes.

As devices become more complex, temperature control also becomes very important, not only in the tester, but also in test interface boards and sockets. Since signal integrity is critical, we believe that our ability to provide solutions that include peripheral equipment is a key point of differentiation for Advantest. We are also investing in turnkey solutions that include these peripherals.

Q: I understand that from the customer's point of view, increased test times and increases in the number of test items due to greater semiconductor complexity will lead to higher test costs. In terms of a future trend, will customers accept this rise in test costs? If they do, how should we think about the balance between cost and added value?

A: You could say that the increase in the number of testers due to the increase in test times has been our main growth driver over the past five years. But we should not assume that this situation will continue forever. 100x increase in complexity does not necessarily mean 100x increase in test demand.

To keep costs under control, it is necessary to work on keeping test times reasonable, providing sufficient test coverage, and keeping test counts reasonable. We strongly feel that we should not become a bottleneck for our customers, so we are taking on the challenge of controlling test times. But with increasing complexity, this is not always easy. Also, in the past, there was a strong perception that test is a cost, but particularly for customers who adopt advanced processes to manufacture HPC devices, test is not a cost, but a very important factor that accelerates Time To Market, Time To Volume, and Time To Quality. I think test has shifted to a role of greater importance.

For this reason, test results are becoming an important parameter for improving yields, not just rejecting defective products. Of course, we have to try to control test times, but we feel that test is becoming a more important contributor to higher semiconductor quality, higher volumes, and early market launch.

Q: As an approximation of times required for test, you commented that the number of total transistors is one metric. For example, smartphone application processors (APUs) do not have that many transistors per chip, but a great many chips of this types are being manufactured. HPC devices, on the other hand, are not manufactured in high quantities,

but they have a very high number of transistors per chip. If one multiplies these numbers and they come out the same, can we assume that tester needs for HPC devices are the same as for smartphone APUs?

A: As an approximation, the equation is not bad, but in reality it is not so simple. The number of transistors is not the only thing that drives complexity. There are many other important factors, such as chiplets and multi-chip packages.

We mentioned the 100x figure earlier, but this is not just the device size and node, but also takes into account the trend for integrating multiple chips in one package. We believe that these factors will complicate test and will drive the demand for testers.

Q: Unlike APUs for smartphones, HPC processors have a long product cycle of 2-3 years. Could customers come up with a way to reduce the number of test items and lower test cost?

A: Possibly, but in the context of device lifetime, for example, early phases are important. During those phases, semiconductor manufacturers strive to improve productivity while learning and mastering various techniques. This means that the need for test is particularly high in the early stages.

In HPC as well, new nodes will be needed in the future, and there are many test needs in the initial stage of ramping up a new node. After a sudden increase, test need growth slows down as the lifetime of the device passes. However, there is always the next device and the next generation, and regarding further growth in test needs, we believe there will be a distribution of test needs across the lifetime of each device.

Q: Regarding increasing complexity, you mentioned integration with software as a particular factor. Is there a risk that EDA tool companies, software companies, etc. will enter the ATE market in the future?

A: That sort of thing is happening, but we do not anticipate much of that kind of competition going forward. We take the opposite view, which envisions a change in the role of test.

For a long time, testers have played the role of detecting failure modes and eliminating them. In the future, we believe test will take on a role of generating knowledge and insights about devices on the path to DFT(Design For Testability). So we see this as more of a future opportunity than a risk.

Note

This document is prepared for those who were unable to attend the information meeting and is intended only for reference purposes. The original content has been revised and edited by Advantest for ease of understanding.

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