Advantest IR Technical Briefing

Test Needs and Solutions in the Memory Semiconductor Market

November 29th, 2023

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NOTE

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Agenda

✓ Memory Tester Business Environment

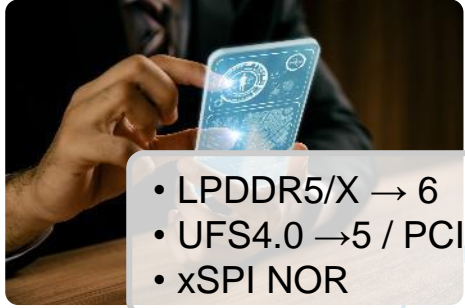✓ Test Needs and Solutions in the Memory Semiconductor Market

Memory Tester Business Environment

Key Applications Driving the Next-Generation Memory Market

Smart phones with higher-definition, AI/LLM* Functionality, Multi-lenses

- LPDDR5/X → 6
- UFS4.0 →5 / PCIe Gen5
- xSPI NOR

* LLM: Large Language Models

Data centers HPC/AI, Cloud

- DDR5
- HBM3E → 4
- GDDR6 → 7
- CXL Memory Module
- PCIe Gen5 SSD

ADAS, Autonomous driving-AI
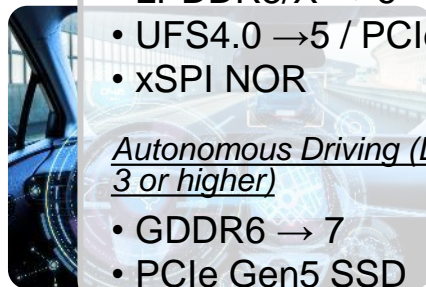
ADAS
- LPDDR5/X → 6
- UFS4.0 →5 / PCIe Gen5
- xSPI NOR

Autonomous Driving (Level 2.x-3 or higher)
- GDDR6 → 7
- PCIe Gen5 SSD

Ultra HD / OLED /Smart TV

- LPDDR5/X
- DDR4 →5
- GDDR6 → 7

AI&XR / e-Sports / Home game consoles
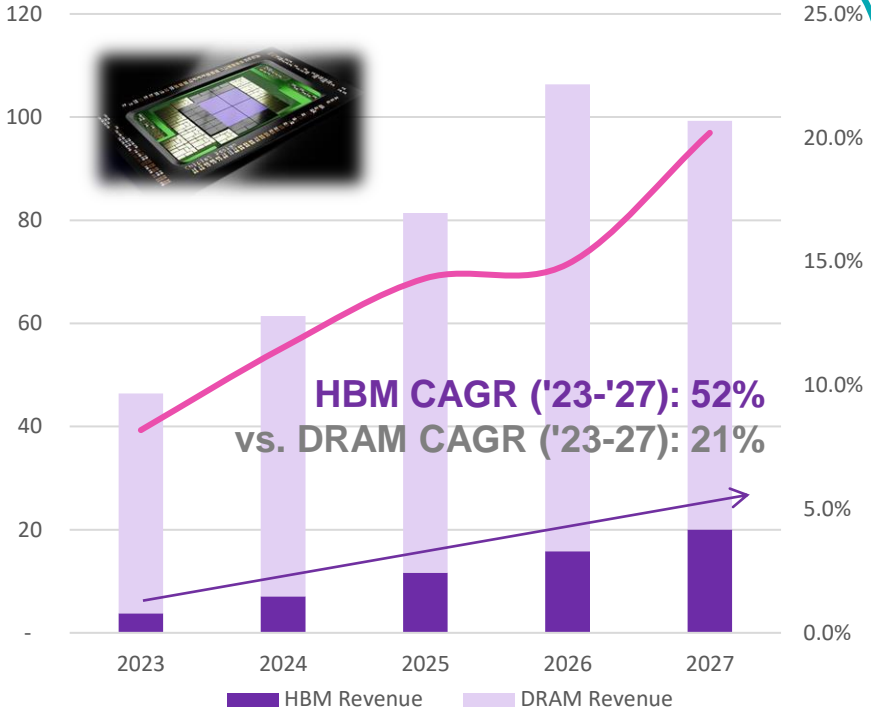
- GDDR6 → 7
- HBM3E → 4
- PCIe Gen5 SSD

Memory market application drivers are data center incl. HPC/AI and mobile

High-performance DRAM for HPC/AI Drives the Market

Holistic Memory Historical Revenue & Forecast

Legend: — DRAM Revenue — NAND Revenue

X-axis: 2005, 2006, 2007, 2008, 2009, 2010, 2011, 2012, 2013, 2014, 2015, 2016, 2017, 2018, 2019, 2020, 2021, 2022, 2023, 2024, 2025, 2026, 2027

Y-axis: $ 0 B, $ 25 B, $ 50 B, $ 75 B, $ 100 B, $ 125 B

HBM & DRAM market revenue

HBM CAGR ('23-'27): 52%
vs. DRAM CAGR ('23-27): 21%

X-axis: 2023, 2024, 2025, 2026, 2027

Legend: HBM Revenue — DRAM Revenue

*CAGR figures have been updated since disclosure was made in Q2 FY2023 financial results presentation by third party research provider.
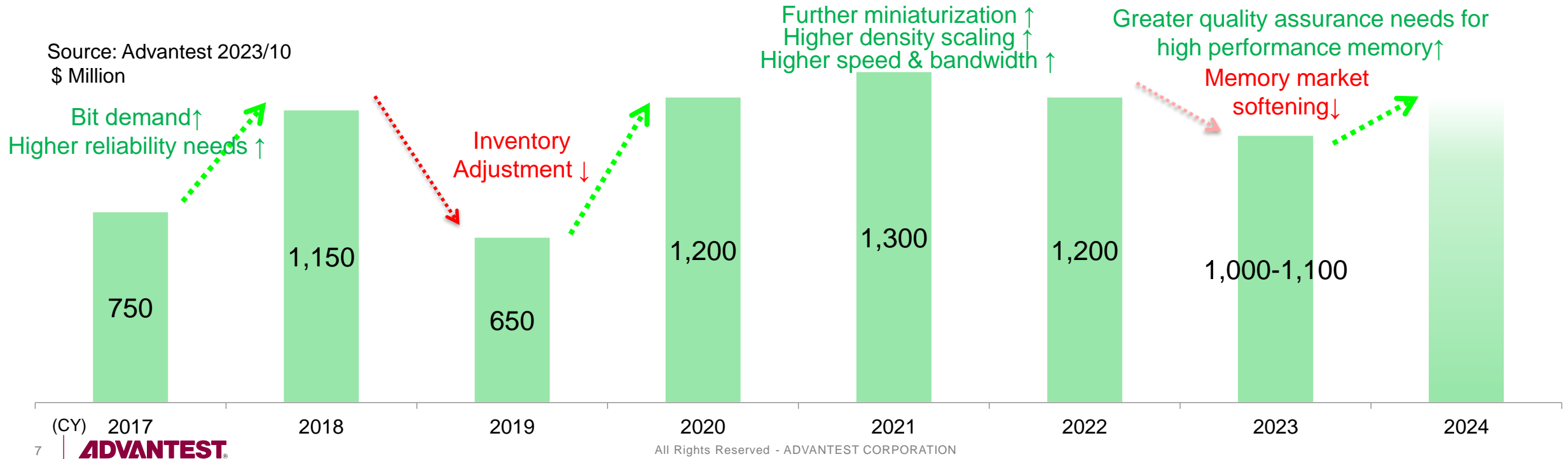
DRAM demand, esp. DDR5 and HBM for HPC/AI servers, is driving the market

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Memory Tester Market Trends

- **Density increase, higher interface speeds**, and **higher reliability assurance** are key determinants of an increase in tester demand

- In comparison with the previous down cycle (2019 vs 2023), the decline caused by the memory market deterioration is somewhat offset by an increase in tester demand for high-performance memory such as HBM and DDR5

- In 2024, the market is expected to expand year-on-year due to a recovery in market conditions and an increasing demand trend for high-performance memory

Memory Tester Market Transforming into a Less-Cyclical Growth Market

Source: Advantest 2023/10
$ Million

Bit demand↑
Higher reliability needs ↑

Inventory Adjustment ↓

Further miniaturization ↑
Higher density scaling ↑
Higher speed & bandwidth ↑

Greater quality assurance needs for high performance memory↑

Memory market softening↓

	2017	2018	2019	2020	2021	2022	2023	2024
(CY)	750	1,150	650	1,200	1,300	1,200	1,000-1,100	

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Core competence to maintain the world's No.1 memory ATE* market share

- **Strong technology capabilities and leadership in the memory test industry**

  - Memory ATE market share in 2022 : 53% (Advantest estimate)

  - First to market optimal test solutions in the high-end market
    Consistently establishing a de facto standard position in the industry
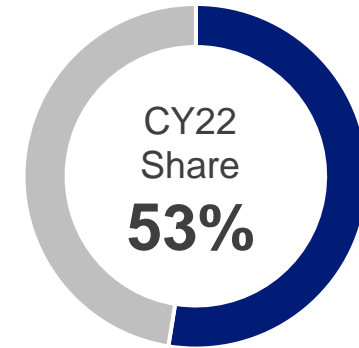
- **Industry's No.1 product portfolio and total solution capabilities**

  - Extensive product portfolio for all test processes
    Competitive advantage through comprehensive solutions including peripherals

  - Enhancing customer's volume production efficiency through
    high product quality that delivers the industry's highest MTBF**

- **The industry's largest and robust customer base**

  - Globally positioned expert engineers with the advanced memory
    testing knowledge and experience accumulated over the years

CY22
Share
53%

Source: Advantest

2023
RANKED 1ST
SUPPLIERS
Tech Insights
CUSTOMER SATISFACTION ™

2023
10 BEST
SUPPLIERS
Tech Insights
CUSTOMER SATISFACTION ™

*ATE: Automated Test Equipment
**: Mean Time Between Failure

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Industry's sole supplier covering all memory test processes

Wafer Level Burn-In	Wafer Level Test	Package Level Burn-in and Core	Final Test Interface

B6700S

T5221

T583X

B6700

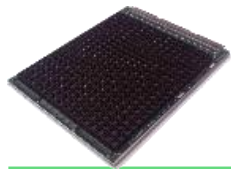**H5620**

T583X

T5503HS2

Full solution line up covering memory test processes

Comprehensive solutions including peripherals

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Integrated solutions for memory device technology evolution & supply growth

Memory test cell "inteXcell" offers extensive test coverage with integration of high throughput handling technology

- Industry-leading test solutions that integrate the memory test, device interface, and auto handler technologies we have accumulated over the years

- InteXcell addresses memory device package testing challenges such as higher density, power savings, and higher interface speed

- Single platform that covers design evaluation to mass production

inteXcell Series 4Cell Configuration

Combines scalability of system configuration with minimized footprint

- Flexibly expand parallelism from 364 to 1,536 DUTs*

  *DUT: device under test

- Footprint reduced to aprx.1/3 of that of conventional products

- Contributing further to production efficiency by controlling each small test cells individually and addressing automation at customers' volume production facilities
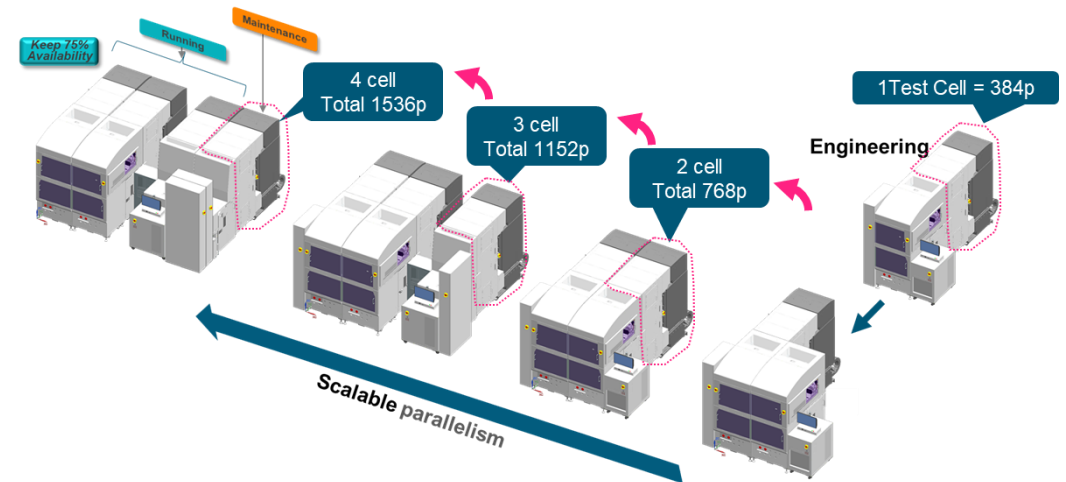
Memory Semiconductor Testing Needs and Solutions

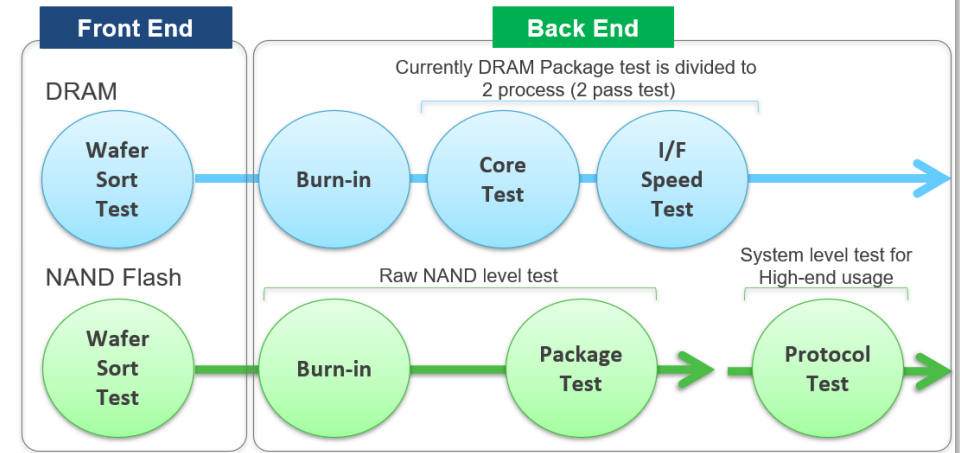# Memory Semiconductor Test Flow and Features

Memory Test Features

- Test flow set up from wafer to package according to test menus and temperature environment

- High parallelism is crucial to optimize throughput according to the technological evolution of memory

- Requirements becoming more rigorous as generation changes have led to higher test speeds and higher reliability assurance needs

Key drivers of memory test/tester demand

- Bit growth (# of chip shipped x memory density) is critical to test demand Transition to advanced processes such as miniaturization of DRAM and increasing 3D-NAND layer count leads to bit growth and longer test time, causing tester demand to grow for each test flow

- Rise in memory data transmission speed creates new demand for high-speed testers DRAM interface speed test process requires testers with new test coverage

- Increase in production volume of high-performance memory semiconductors for AI/HPC with high reliability requirements For HBM, tester demand increases due to more elaborate testing and additional test insertions post stacking driven by higher reliability requirements alongside adoption of advanced packaging
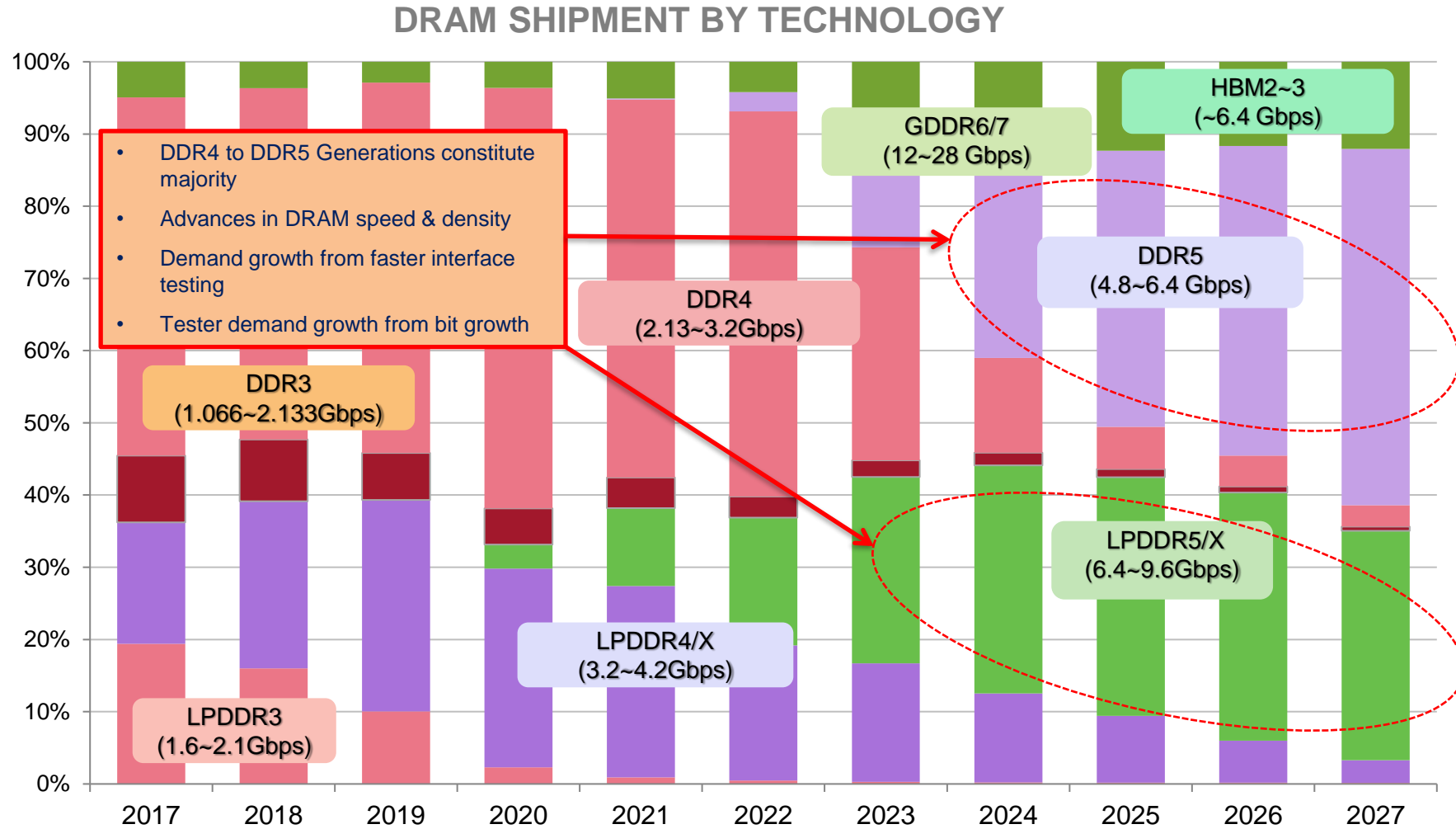
Memory Device Test Flow

Front End — DRAM — **Back End**

Currently DRAM Package test is divided to 2 process (2 pass test)

DRAM: Wafer Sort Test → Burn-in → Core Test → I/F Speed Test

System level test for High-end usage

NAND Flash: Wafer Sort Test → Burn-in → Package Test → Protocol Test

Raw NAND level test

Test needs and technology challenges for next generation memory

Wafer Level Burn-in	Wafer Level Sort	Package Level Core and Burn-in	Package Level High speed Interface
• High Functionality • High Power	• Massive Parallelism 1000→2000→3000 DUTs* • High Speed Probing 2.4Gbps → 5Gbps< • High Power, Multi-Power Supply	• High Power • Thermal Control Coverage -40 °C to +150°C • High Functionality	• Massive Parallelism 512 DUTs*, 768 DUTs* • High Frequency 9Gbps, >12Gbps • High Precision

*DUT: device under test

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DRAM Interface Trend Forecast

DRAM SHIPMENT BY TECHNOLOGY

- DDR4 to DDR5 Generations constitute majority
- Advances in DRAM speed & density
- Demand growth from faster interface testing
- Tester demand growth from bit growth

HBM2~3 (~6.4 Gbps)

GDDR6/7 (12~28 Gbps)

DDR5 (4.8~6.4 Gbps)

DDR4 (2.13~3.2Gbps)

DDR3 (1.066~2.133Gbps)

LPDDR5/X (6.4~9.6Gbps)

LPDDR4/X (3.2~4.2Gbps)

LPDDR3 (1.6~2.1Gbps)

# High-bandwidth memory HBM supporting social implementation of gen. AI

Rapid spread of gen. AI such as ChatGPT & advanced LLMs
Sharp demand acceleration of for high-performance AI modules (GPU+HBM)
(HBM market: 52% CAGR projected over 2023-2027)

What is HBM (High Bandwidth Memory)?

- A type of 3D stacked memory technology. Higher bandwidth and density scalability than conventional 2D memory

- Challenges exist for advanced packaging such as 2.5D/3D with increased manufacturing costs and thermal control. Used primarily in high-performance HPC/AI computing

- Latest HBM3 offers 12 times higher density and 13 times higher bandwidth than GDDR6
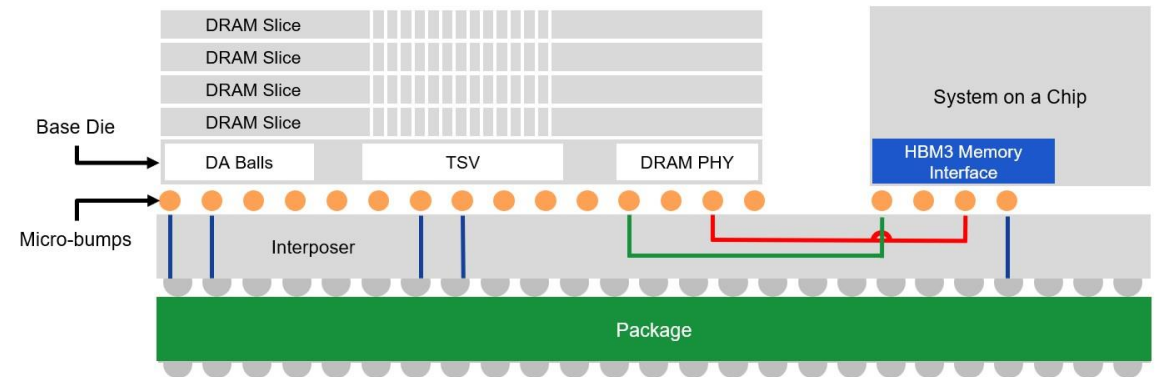

HBM3 Memory Interface (Source: Rambus Inc.)

> **High market growth rate is expected as GPUs with high parallel processing with thousands of cores or more and HBM with its optimal configurations are essential for AI technology, which requires enormous computing power**

HBM Technology Trends and Outlook

Rapid expansion from HBM3 to HBM4 generation over the next 5 years, led by AI modules for data centers

HBM Shipments (m Gb)
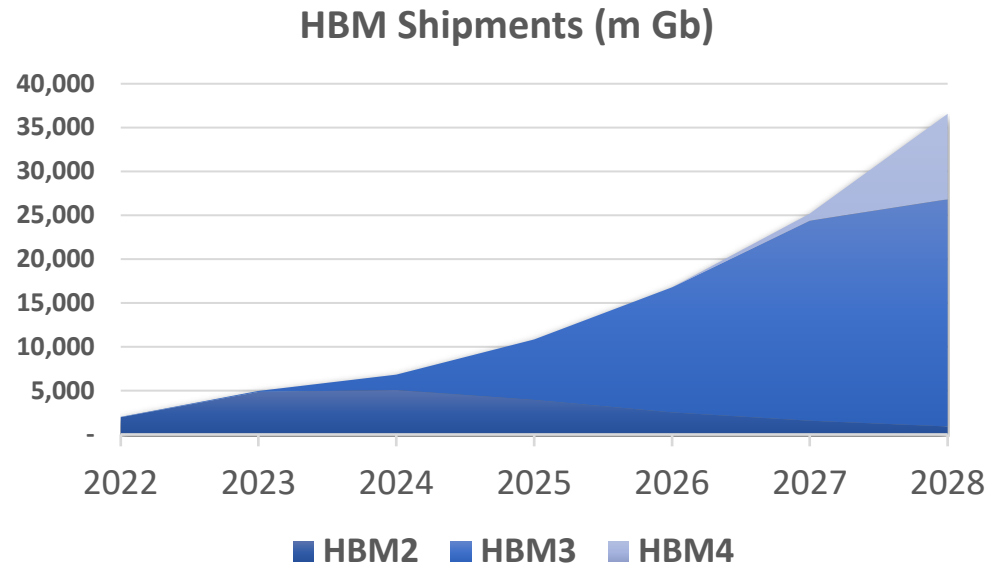
Source by Yole, YINTM23310Q3-DRAM_Market_Monitor_Q3

- HBM CAGR of 49% from 2023-2028 (bit base)
- Rapid share expansion of HBM3 (incl. enhanced versions) after 2024
- New process development, addressing issues such as thermal and cost, is expected for the next generation HBM

Interface speed, bandwidth, stack count, and density expected to double with each generation
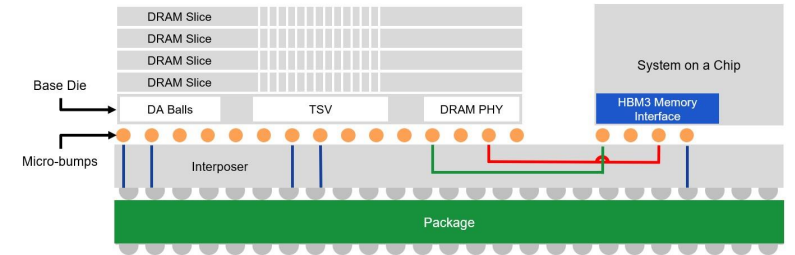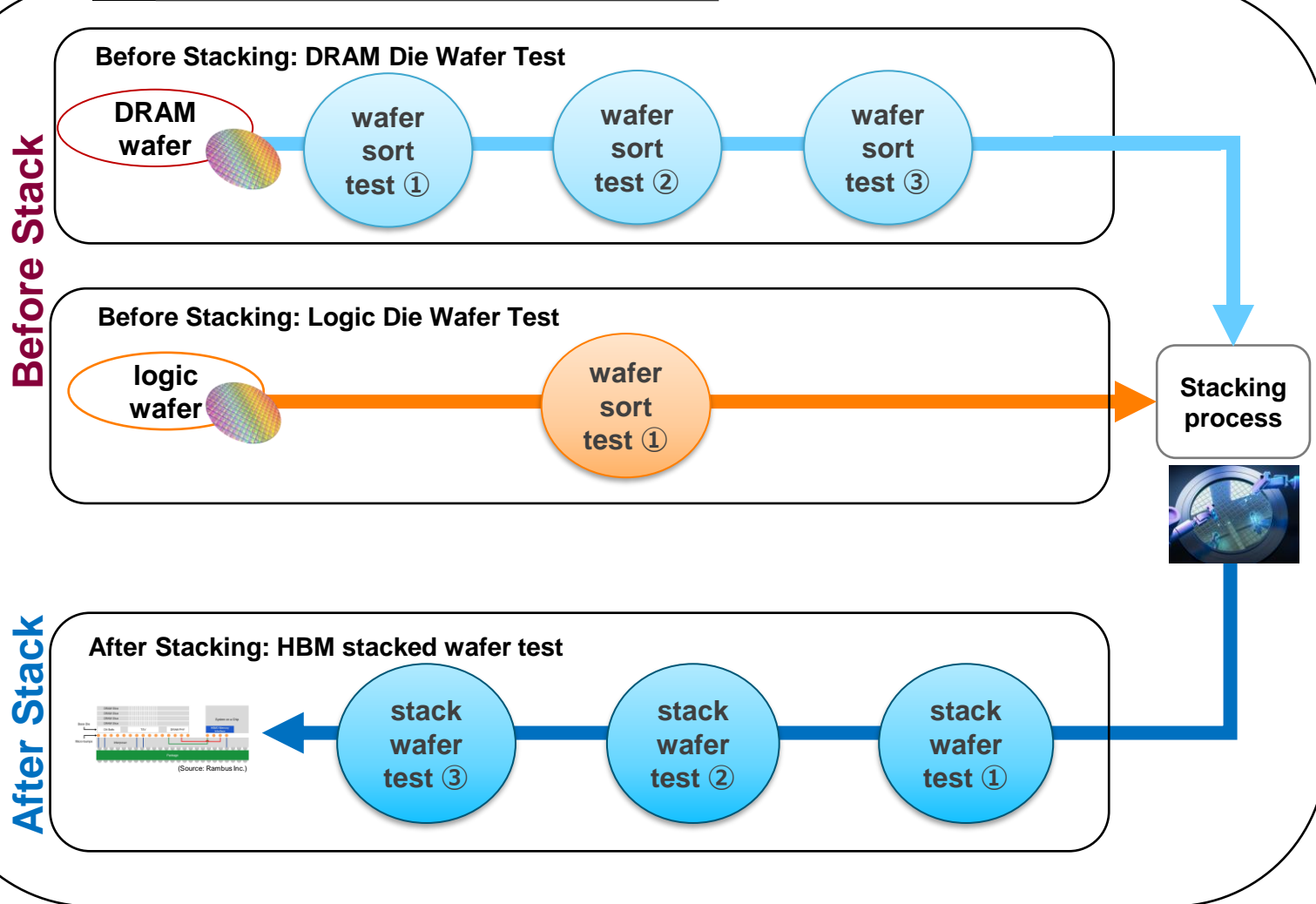
Performance Comparison by HBM Generation

	HBM2E	HBM3	HBM4
Memory bandwidth	460GB/s	>820GB/s	>1.5TB/s
Density per die	8/16Gb	16/24Gb	24/32Gb
Stack count	4, 8	8, 12	8, 12, 16
IO Speed	3.2 Gbps	>6.4Gbps	TBD

Includes Advantest Marketing Estimation

- Bandwidth performance growing multiple-fold from HBM2E, HBM3, its enhanced versions, and to HBM4 generation
- Memory density increases as the HBM stack count changes to 4-8-12-16 stacks, along with the miniaturization of the individual die

Current HBM testing process and issues

■ HBM testing process(illustrative)

Before Stack

Before Stacking: DRAM Die Wafer Test

DRAM wafer → wafer sort test ① → wafer sort test ② → wafer sort test ③

Before Stacking: Logic Die Wafer Test

logic wafer → wafer sort test ① → **Stacking process**

After Stack

After Stacking: HBM stacked wafer test

stack wafer test ③ ← stack wafer test ② ← stack wafer test ①

(Source: Rambus Inc.)

HBM3 Memory Interface (Source: Rambus Inc.)

■ Test Challanges

- Each new generation leads to increased density & stacks (8->12->16 stacks)
  ➡ Longer test time
- Each new generation leads to higher interface speed
  ➡ Higher test speed/increased load on peripheral circuits
- Increase in power supply & current capacity
  ➡ Tester scalability, impact on parallelism
- Yield impact before and after HBM stacked wafer dicing (e.g., die level test)

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Business opportunities for memory testers arising from gen. AI

Increase in high-performance memory incl. HBM / DDR5

HBM & DRAM market revenue

HBM CAGR ('23-'27) : 52%
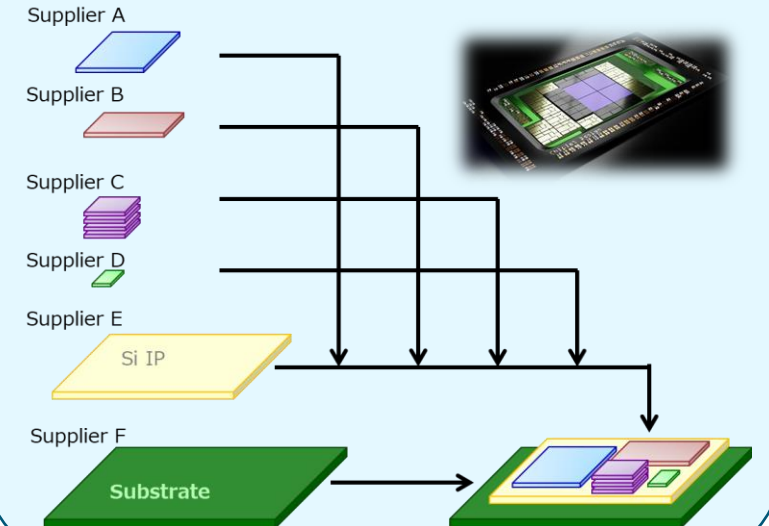**vs. DRAM CAGR ('23-27) : 21%**

Legend: ■ HBM Revenue ■ DRAM Revenue
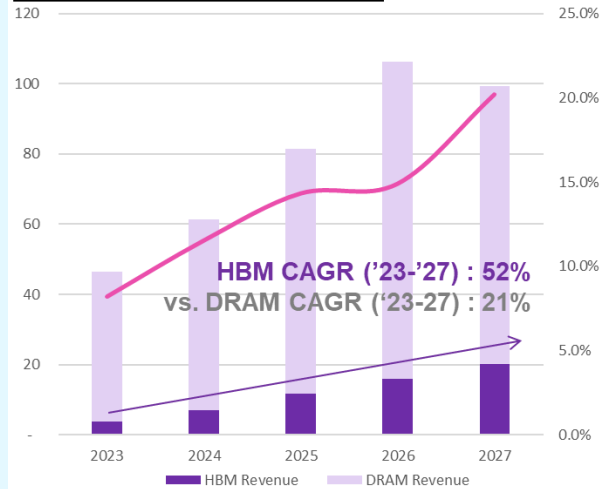
Source: Omdia DRAM Market Tracker Q2,23.
Results are not an endorsement of Advantest. Any reliance on these results is at the third-party's own risk

*CAGR figures have been updated since disclosure was made in Q2 FY2023 financial results presentation by third party research provider.

Increase in advanced packages incl. 2.5D/3D

Supplier A
Supplier B
Supplier C
Supplier D
Supplier E — Si IP
Supplier F — Substrate

Rising quality assurance requirements due to higher functionality and complexity growth

ENHANCED — Wafer Sort Test — ENHANCED
ENHANCED — Package Test — ENHANCED

HBM
DDR5

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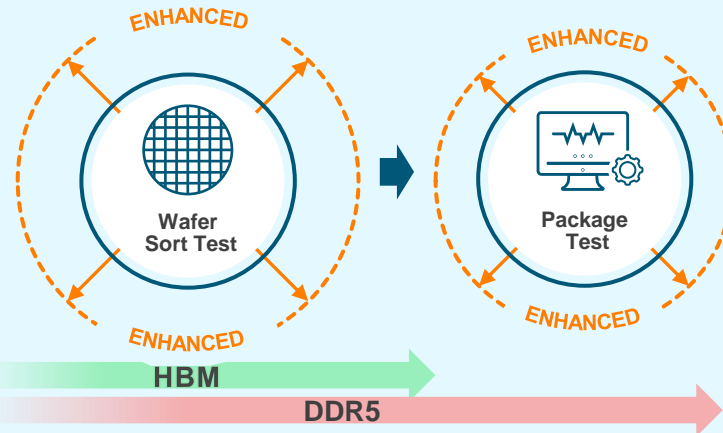
Memory Tester Business Environment and Growing Test Demand

Continued increase in memory performance & density in all areas

- Data centers incl. HPC/AI and mobile to drive the memory market
- Rapid adoption of gen. AI and advanced LLMs increases demand for high-performance AI modules (GPU+HBM)
- In particular, high-performance memory such as HBM and DDR5 to drive the market

Semi Production Increases "Capacity Buy"

Memory semiconductor production volume to increase due to broadening of applications

Tester demand to grow for HBM in response to expanding production plans by customers

Semi Technology Evolution "Technology Buy"

Bit growth accelerated by transition to advanced processes, causing test time to increase

Increasing memory speeds create demand for faster interface test

Higher quality & reliability needs "Quality Buy"

Higher quality assurance needs for high-end memory leads to more elaborate testing, causing test time to increase

Supporting the technological evolution & growing demand of memory devices with "Tested by Advantest," contributing to the realization of "safety, security, & comfort" of society